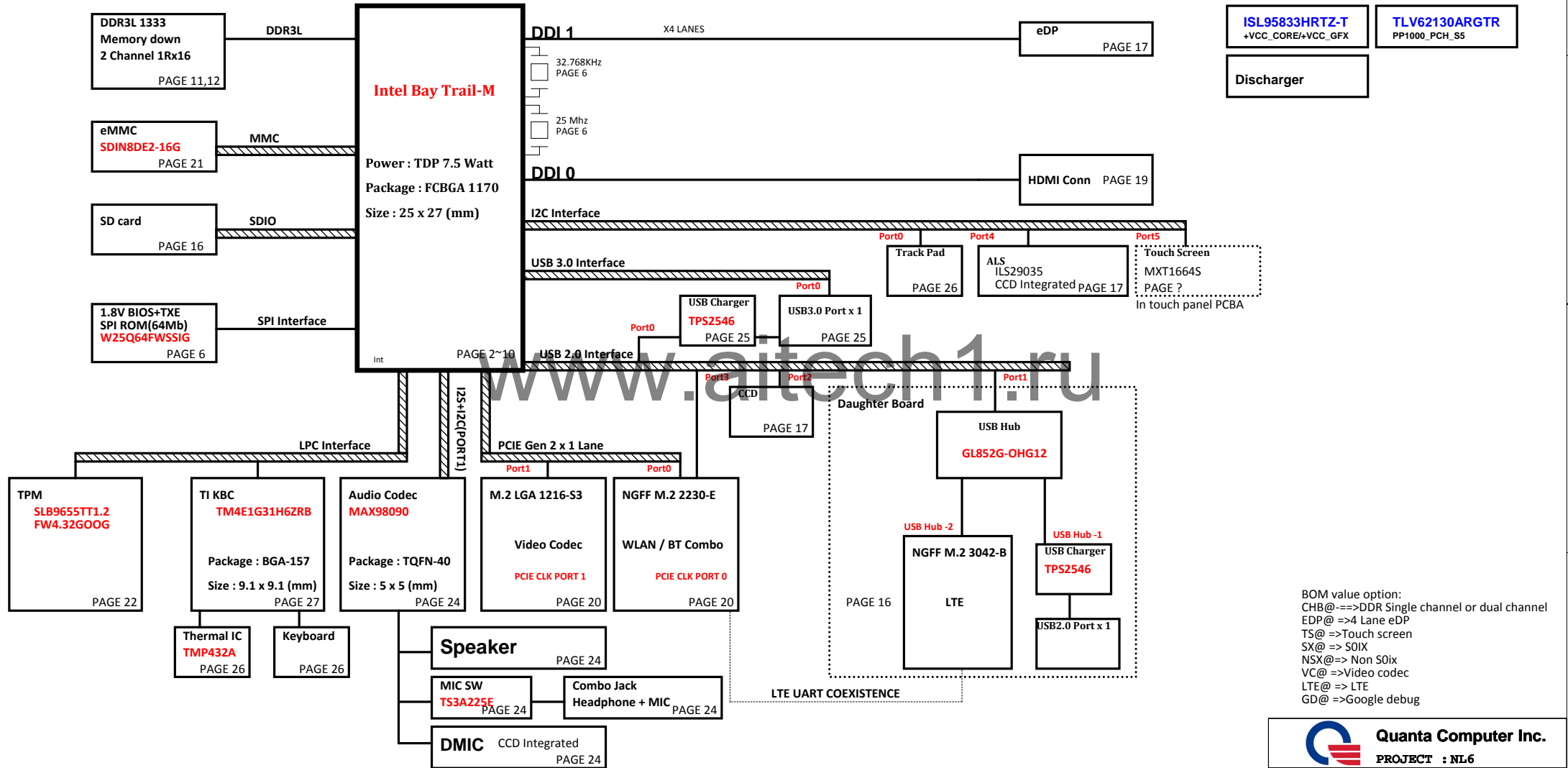


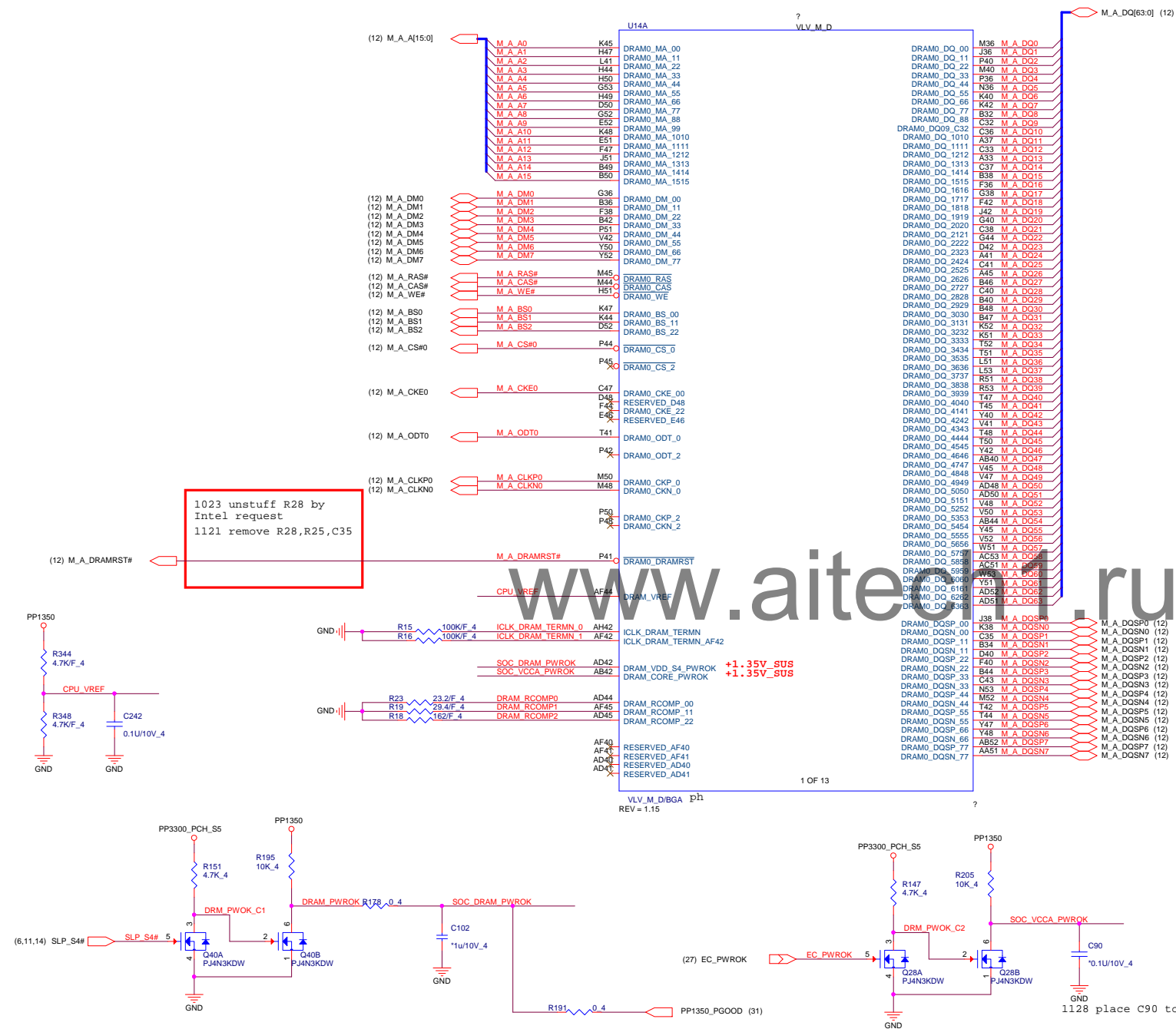
Intel Bay Trail-M Platform Block Diagram

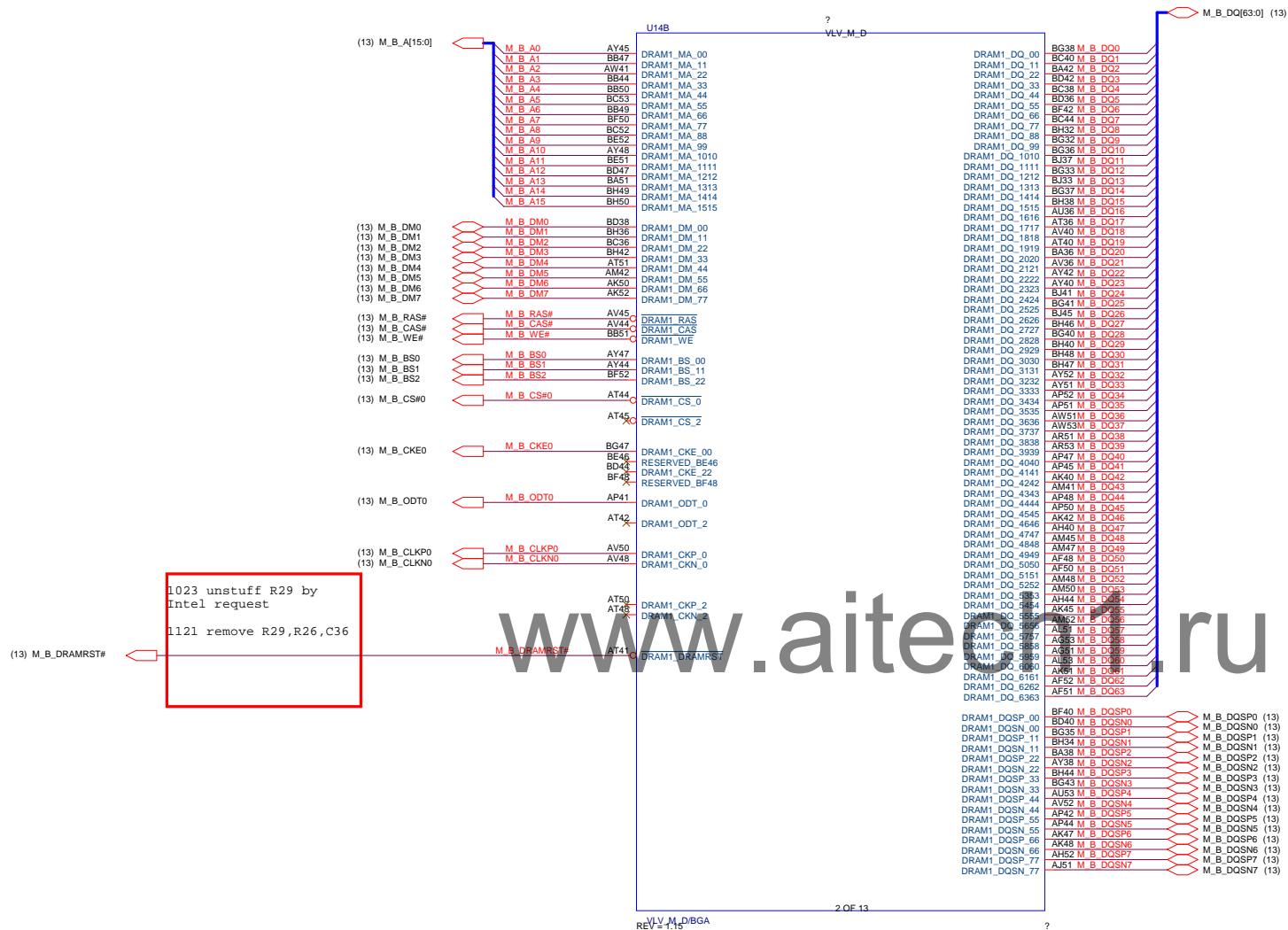
SKUA QC N2930
Up to 1.83 GHz SR1SG(FCBGA) P/N: AJ0QG9UUT01
SKUB DC N2830
Up to 2.17 GHz SR1SG(FCBGA) P/N: AJ0QG9VUT01

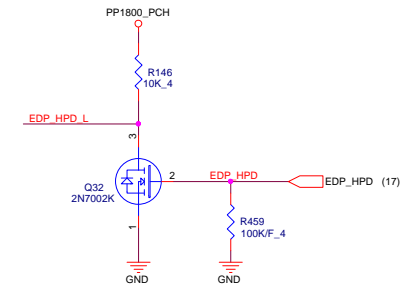


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Intel Block Diagram
Date: Friday, April 25, 2014 Sheet 1 of 41





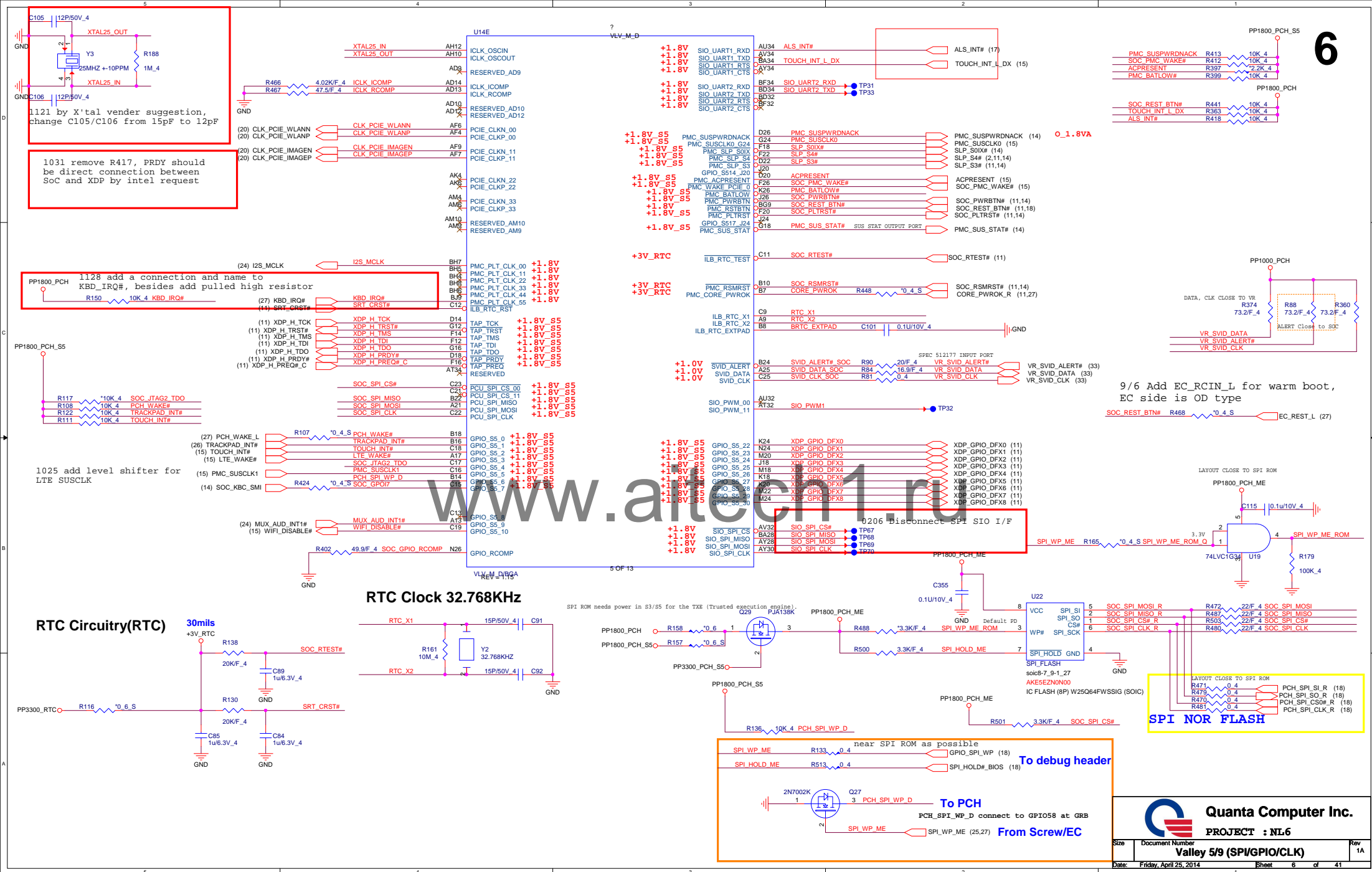


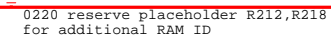
| Pin Name | Strap description | Sampled | Configuration | Note |
|---------------|----------------------------|---------|---|--------------------------------|
| GPIO_SO_SC_56 | Top Swap (A16 Override) | PWROK | 0 = Top address bit is unchanged 1 = Top address bit is inverted | (7) GPIO_SO_SC_56 |
| LPE_I2S2_FRM | BIOS Boot Selection | PWROK | 0 = LPC 1 = SPI | (5) I2S_LRCLK |
| GPIO_SO_SC_65 | Security Flash Descriptors | PWROK | 0 = Override 1 = Normal operation | (5) 2S_DOUT |
| DDI0_DDCDATA | DDI0 Detect | PWROK | 0 = DDI0 not detected 1 = DDI0 detected | Pull up +1.8V at HDMI side |
| DDI1_DDCDATA | DDI1 Detect | PWROK | 0 = DDI0 not detected 1 = DDI0 detected | |
| GPIO_SO_NC_13 | | | | |

| |
|---|
| 1029 unstuff R128, using SoC internal PU |
| 1029 unstuff R372, using SoC internal PU |
| 1115 stuff R372, system can't boot if un-stuff R372 on protol.5 board, need intel double confirm before proto2 |

| | | |
|------|-------------------------------------|--|
| 1029 | unstuff R386, using SoC internal PU | |
| 1115 | stuff R386, it is required for eDP | |







Proto1/1.5 stage use H2G & H4G
1212 add new RAMID 101 for single channel SKU



0220 R392,R389,R71,R65 need always to be stuffed even if w/o TS SKU



1101 add option BOM R446,R449 for
EC CLK for power saving by Intel
request



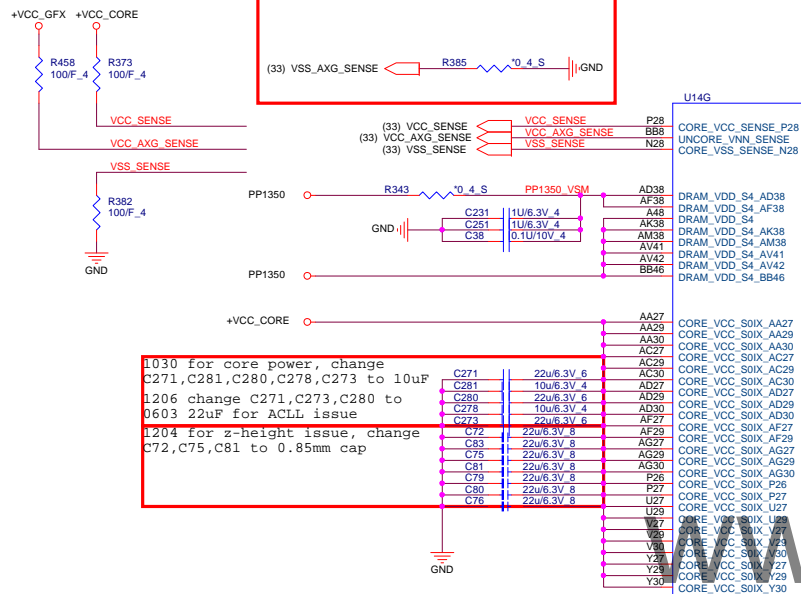
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| | | |
|-------|---------------------------------|---------------|
| Size | Document Number | Rev |
| | Valley 6/9 (USB/LPC/I2C) | 1A |
| Date: | Friday, April 25, 2014 | Sheet 7 of 41 |

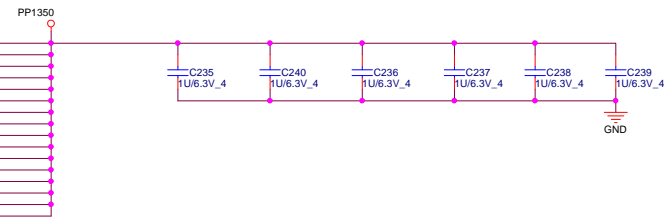
1031 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE
1031 for layout, add 0hm between GND and VSS_AXG_SENSE

(33) VSS_AXG_SENSE \leftarrow R385 \rightarrow 0.4 S \rightarrow GND



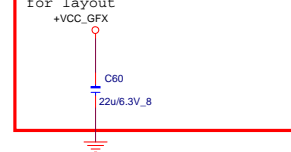
REV = 1.15 1031 remove TP44 and TP35 for GND vias adding

U14G
CORE_VCC_SENSE_P28
UNCORE_VNN_SENSE
CORE_VSS_SENSE_N28
DRAM_VDD_S4_BD49
DRAM_VDD_S4_BD52
DRAM_VDD_S4_BD53
DRAM_VDD_S4_BF44
DRAM_VDD_S4_BG51
DRAM_VDD_S4_BJ48
DRAM_VDD_S4_C51
DRAM_VDD_S4_D44
DRAM_VDD_S4_F49
DRAM_VDD_S4_F52
DRAM_VDD_S4_F53
DRAM_VDD_S4_H46
DRAM_VDD_S4_M41
DRAM_VDD_S4_M42
DRAM_VDD_S4_V38
DRAM_VDD_S4_Y38
UNCORE_VNN_S3_AA24
UNCORE_VNN_S3_AC22
UNCORE_VNN_S3_AC24
AD22
AD24
AF22
AF24
AG22
AG24
AJ22
AJ24
AK22
AK24
AK25
AK29
AK30
AK32
AK33
AKM22



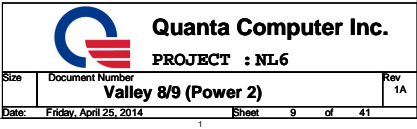
1030 for Gfx power, change C266,C289,C290 to 10uF and add 2 caps 10uF
1206 change C266,C311,C315 to 0603 22uF for ACLL issue

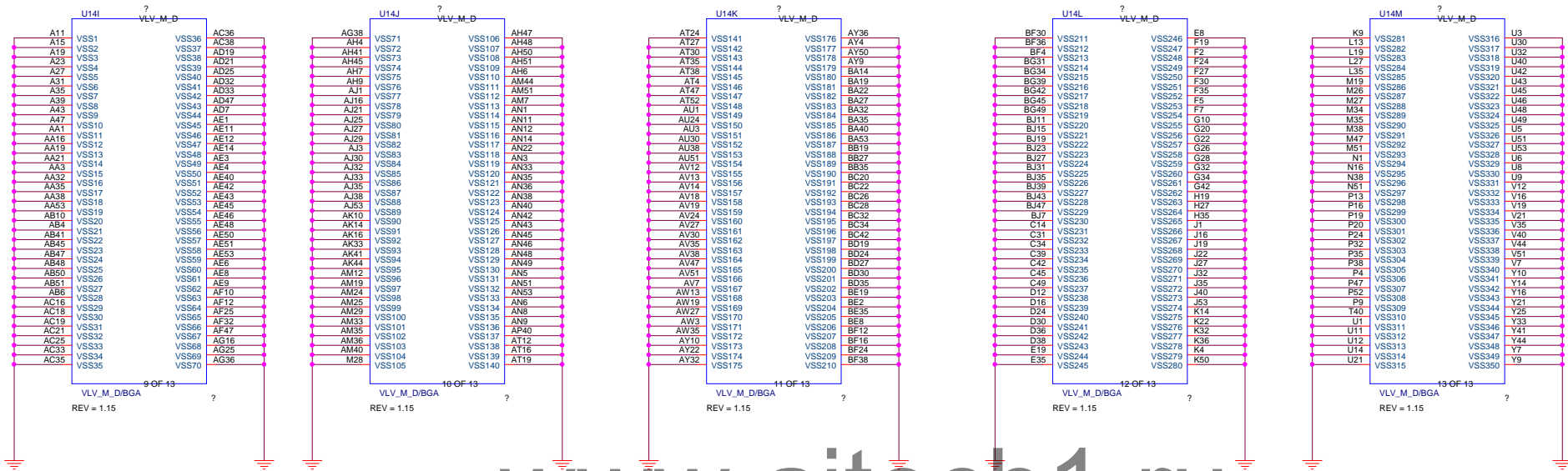
1030 change C60 power netname for layout



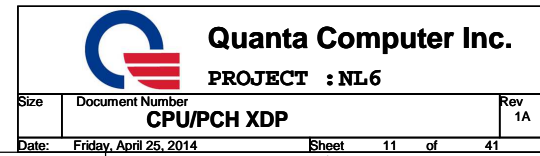
Quanta Computer Inc.
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| | | |
|-------|------------------------|---------------|
| Size | Document Number | Rev |
| | Valley 7/9 (Power 1) | 1A |
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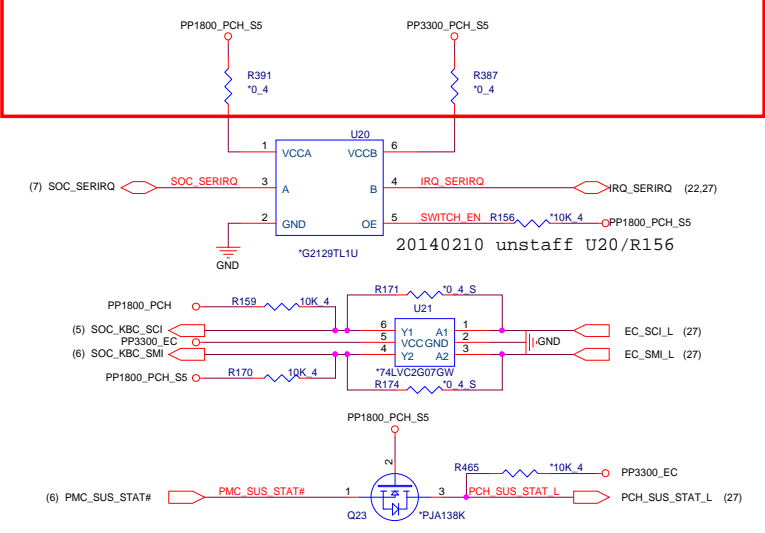


11

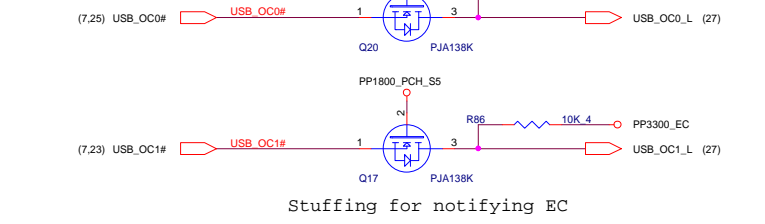


PWRON SEQUENCE

9/6 EC table says SERIRQ is OD pin, reserve for debugging
 1128 remove R166, because SERIRQ of TPM needs 3V
 1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging
 20140210 unstuff R387/R391

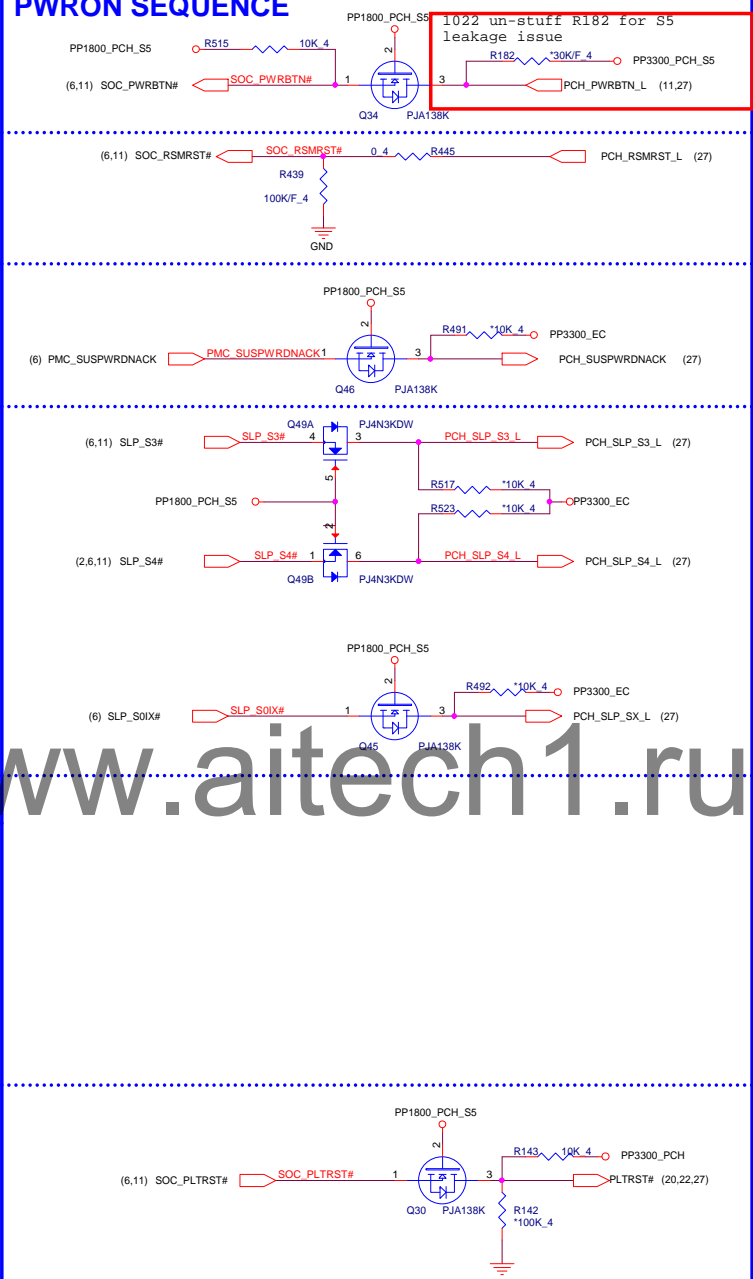


USB OC



Stuffing for notifying EC

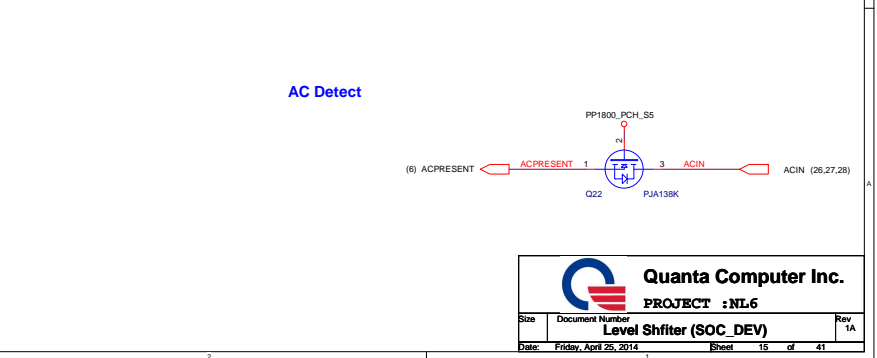
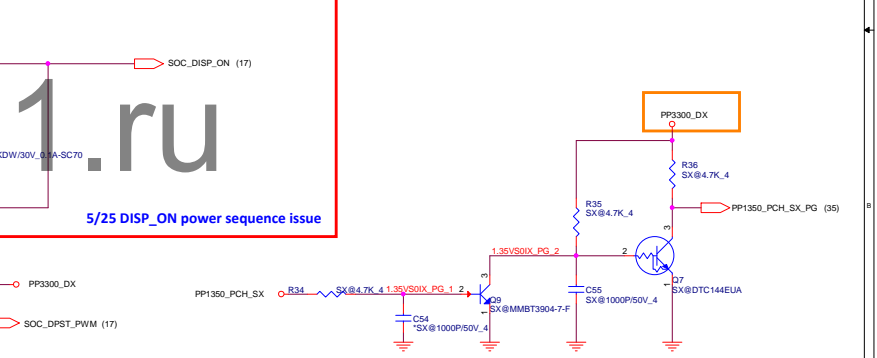
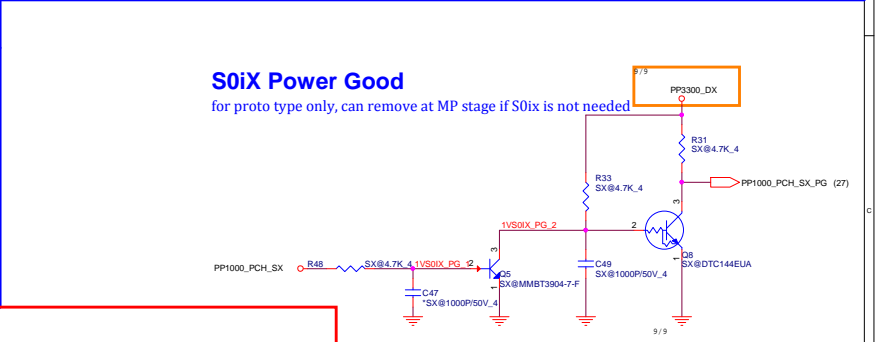
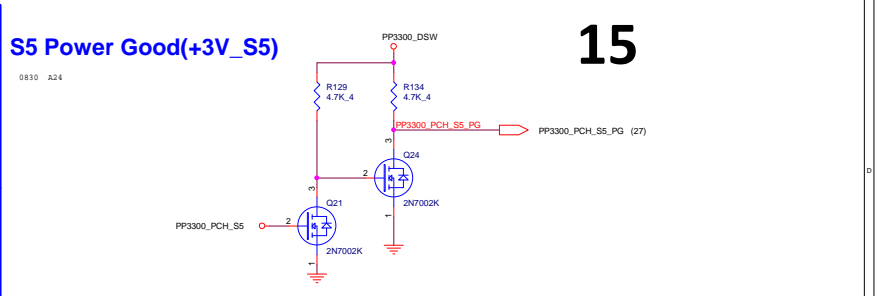
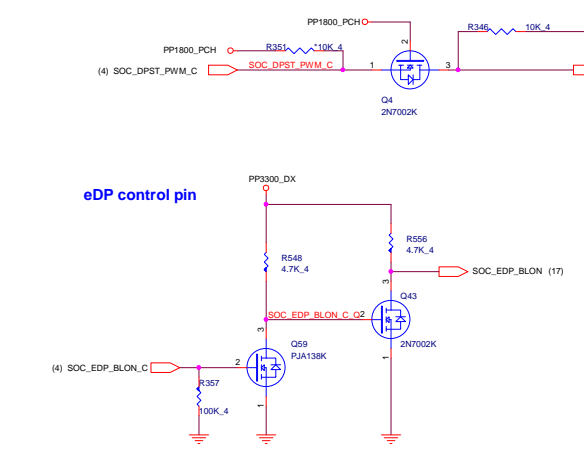
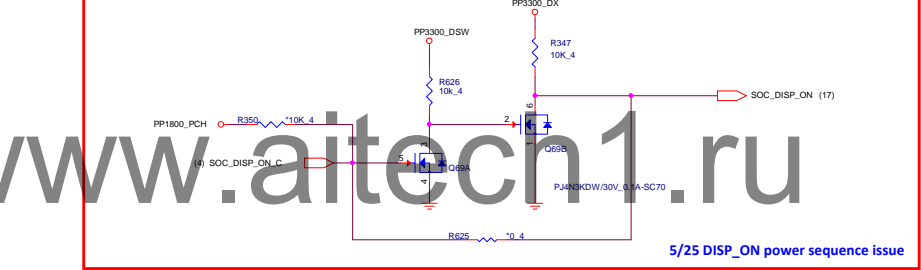
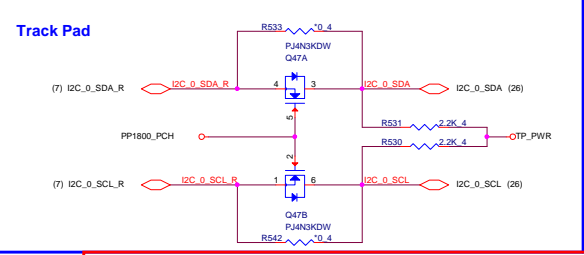
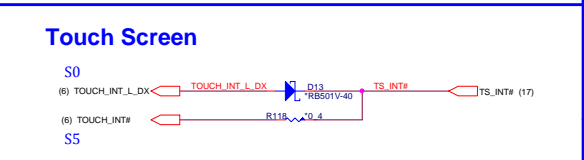
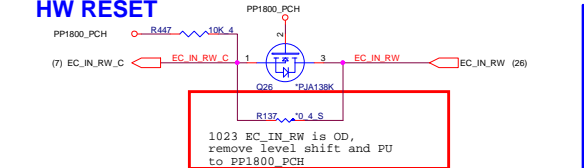
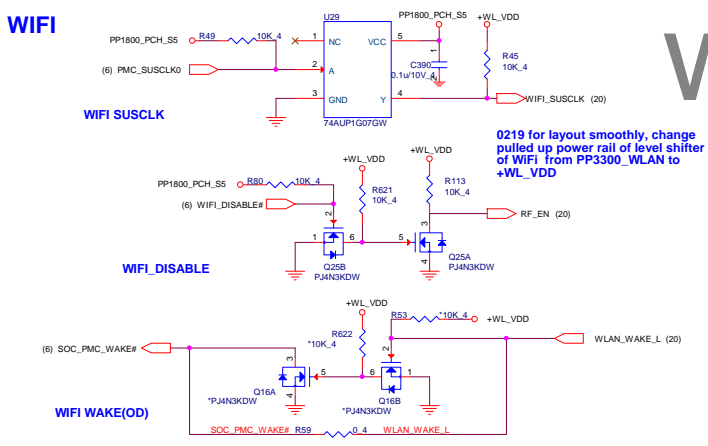
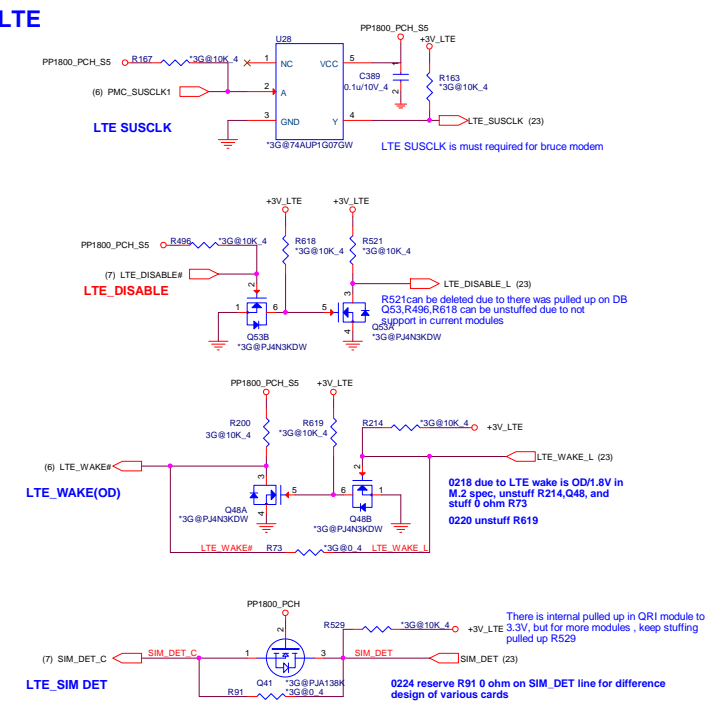
PWRON SEQUENCE



0128 change power rail of Q35,Q36,Q37,Q44 from PP1800_PCH_S5 to PP1800_PCH for PP1800_PCH leakage issue in S3 mode

0206 remove/delete SPI_SIO Interface, Q35,Q36,Q37,Q44,R486,R484,R485,R483,R426,R429,R427,R428

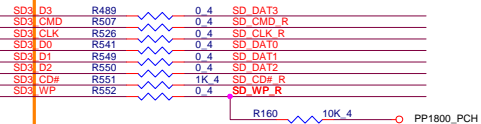
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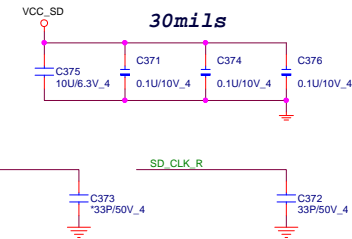
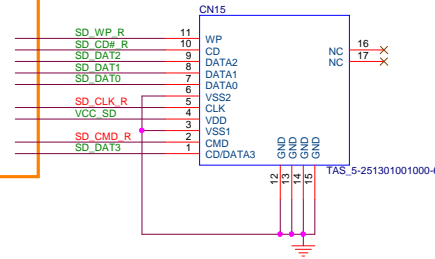
SD/MMC CARD READER CONNECTOR (MMC)

1205 the damping of SDIO change to 0 ohm by Intel request
 1205 add PU for SDIO WP by Intel request
 1205 R551 changes to 1K to isolate SD socket and servo/SoC
 1205 SD3_WP is 1.8V power rail in SoC, change external Pulled up power well of SD3_WP to 1.8V power

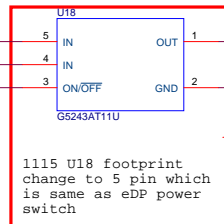
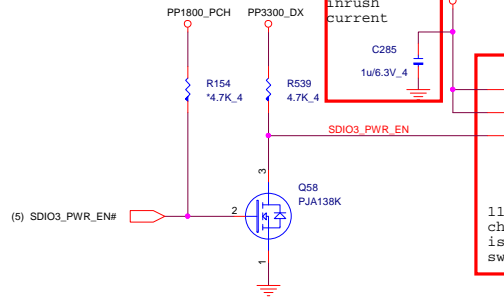
(5) SD3_D3
 (5) SD3_CMD
 (5) SD3_CLK
 (5) SD3_D0
 (5) SD3_D1
 (5) SD3_D2
 (5,18) SD3_CD#
 (5) SD3_WP



This is full size SD card

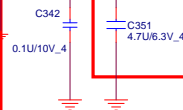


1202 add C285 for U18 input inrush current



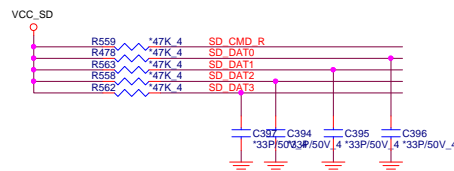
VCC_SD

1101 correct C351 footprint



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1211 add pulled up resistors on SDIO data/cmd lines
 1212 all pulled up resistors of SDIO data/cmd to be un-stuffed



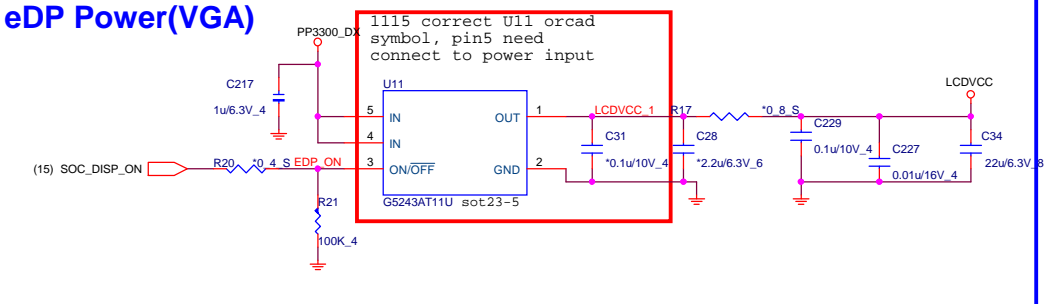
Quanta Computer Inc.

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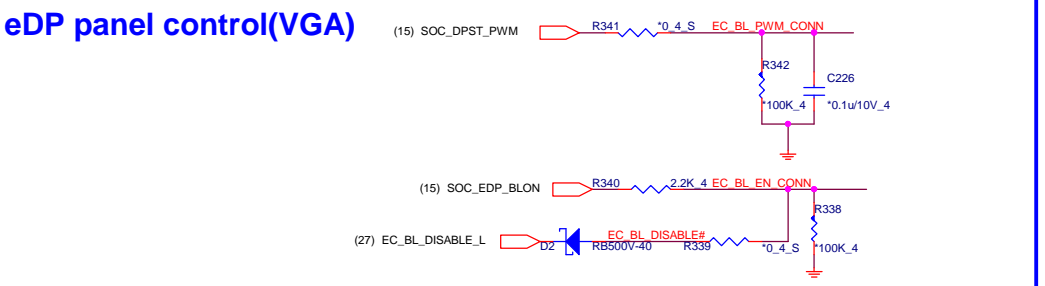
SDIO CardReader

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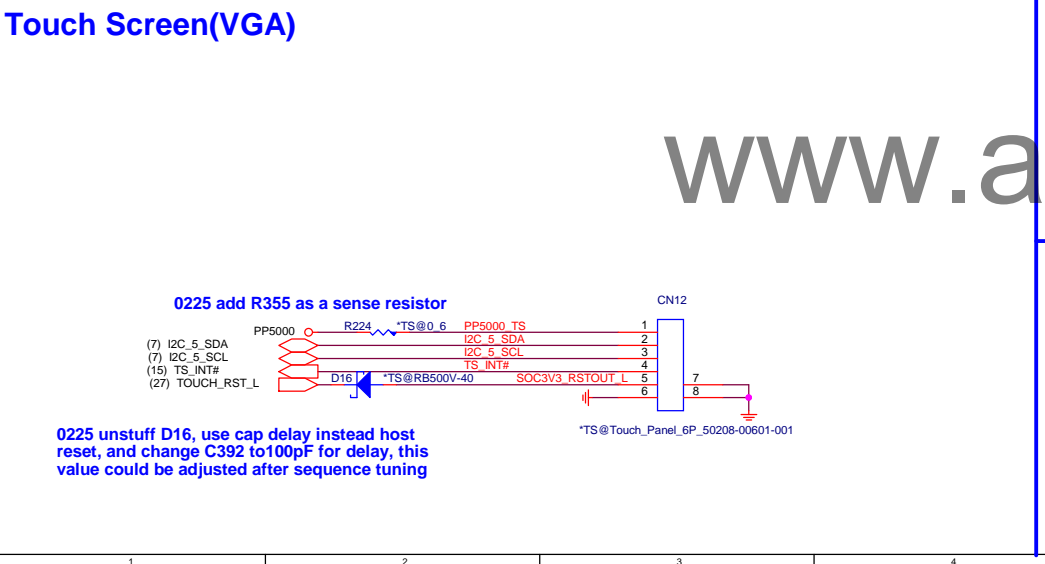
eDP Power(VGA)



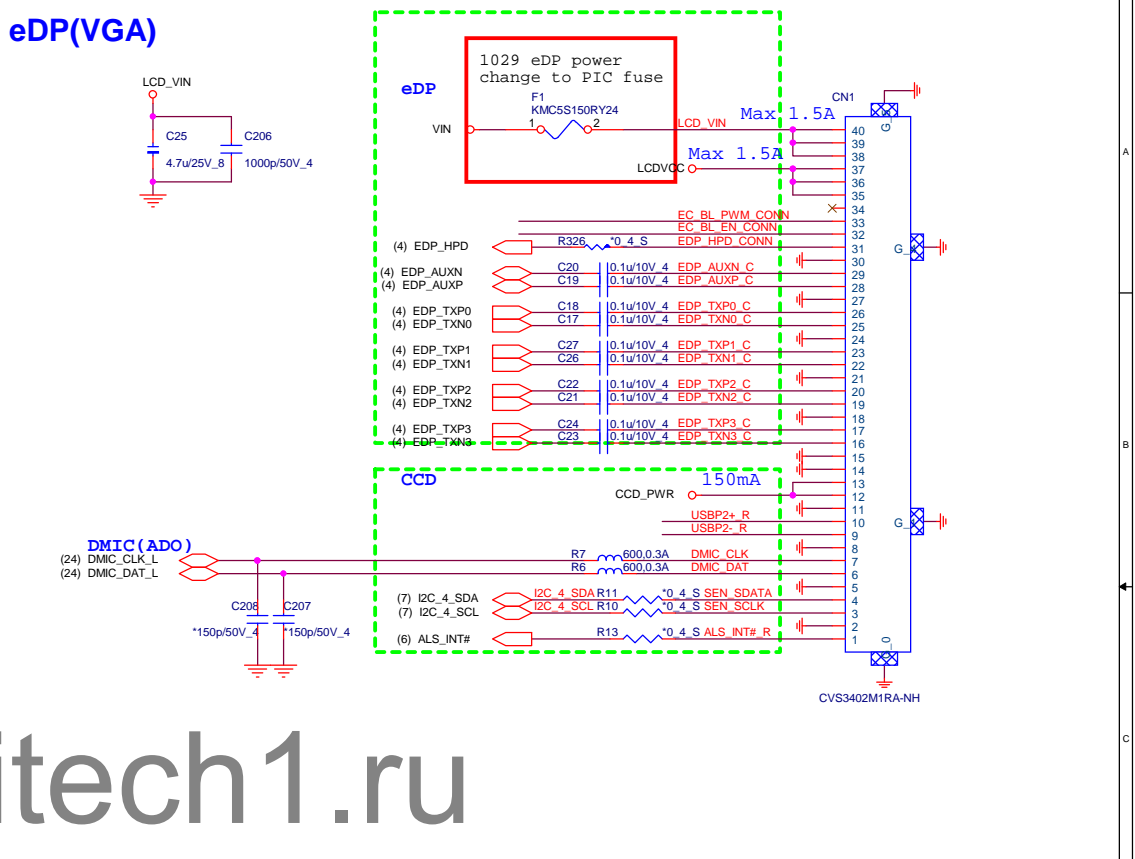
eDP panel control(VGA)



Touch Screen(VGA)



eDP(VGA)



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GOOGLE Debug Port(MPC)

50 pin BTB is **MUST**, don't use 42 pin

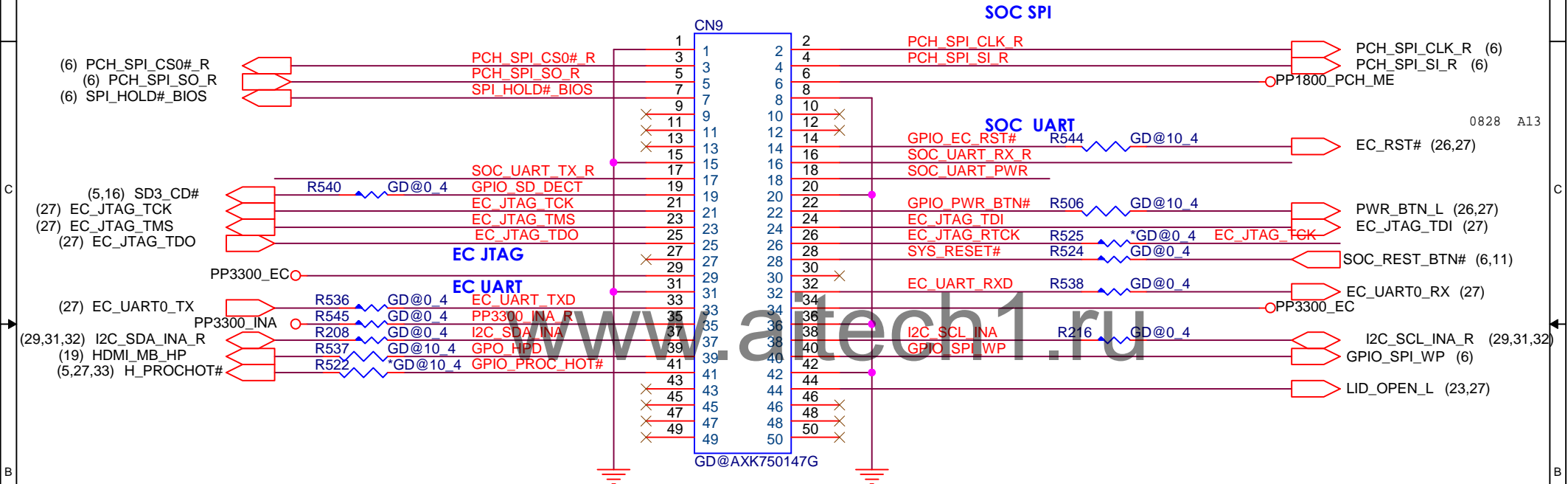
Socket part number AXK750147G

```
PIN7  OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
```

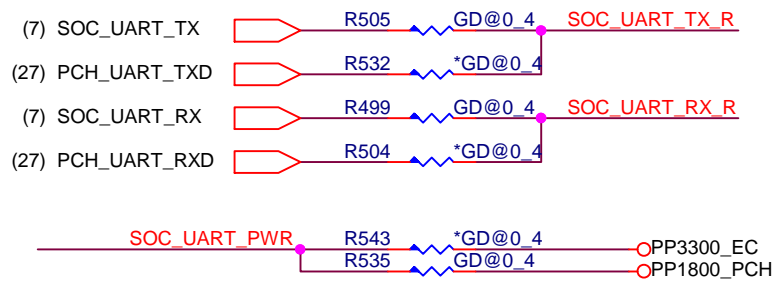
| | |
|-------|----|
| PIN39 | OD |
| PIN41 | OD |
| PIN43 | OD |
| PIN44 | OD |
| PIN45 | OD |
| PIN46 | OD |
| PIN47 | OD |
| PIN48 | OD |

PIN49 OD
PIN50 OD

18

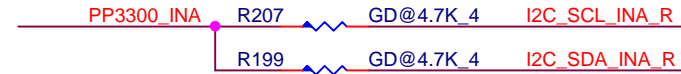


1021 change footprint and PN



9/6 using optional instead of level shifted, default is from SoC

9/13 add pull up



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|------|-----------------|
|------|-----------------|

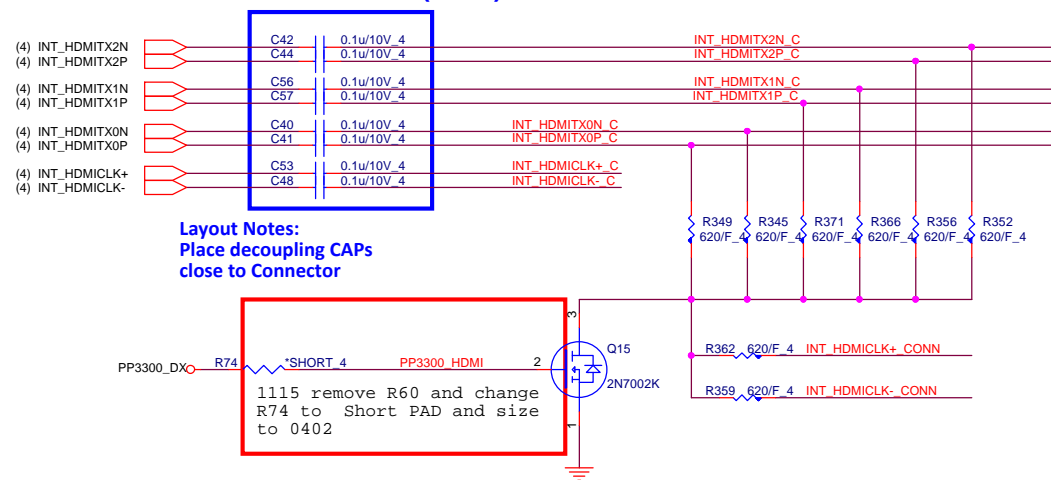
Google Debug

Rev
1A

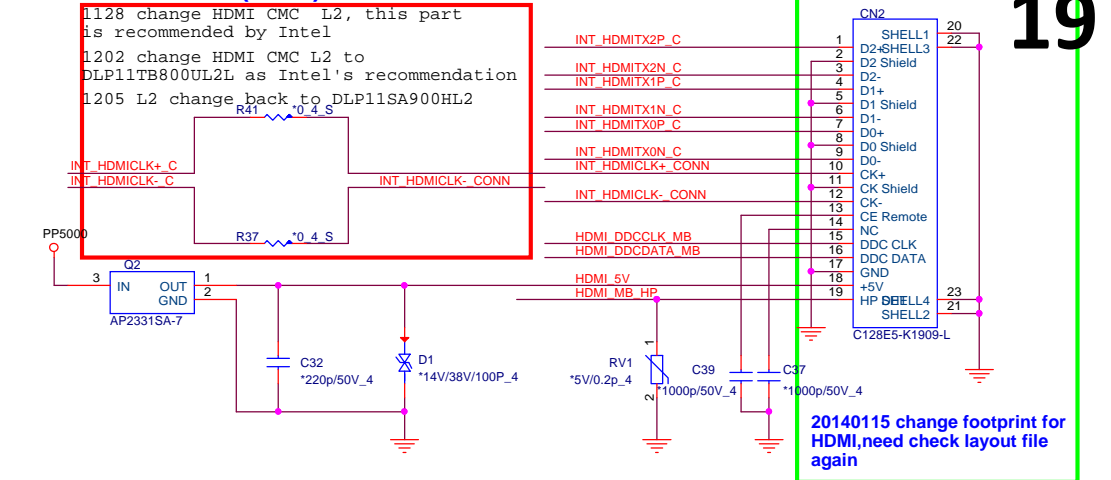
Date: Friday, April 25, 2014

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HDMI Cost Reduced level shift (HDM)

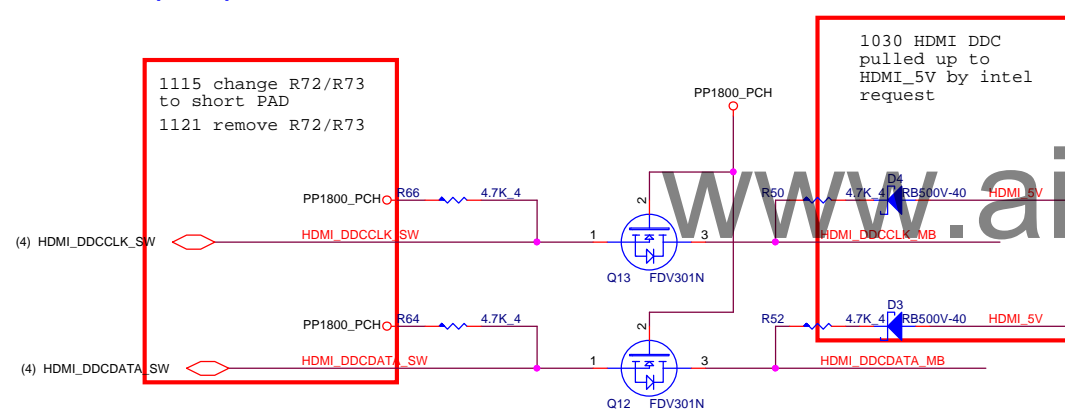


HDMI connector (HDM)

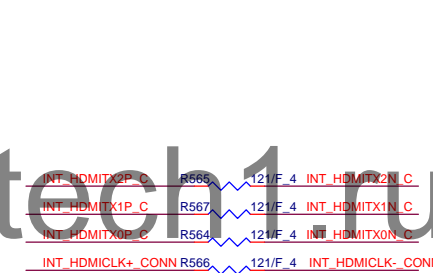


19

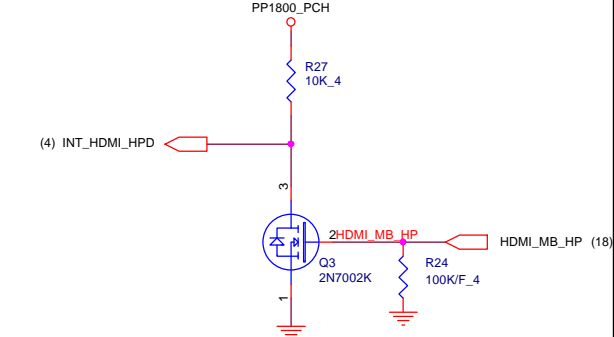
HDMI DDC (HDM)



EMI



HDMI-detect (HDM)



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|------|-----------------|-----|
| | HDMI | 1A |

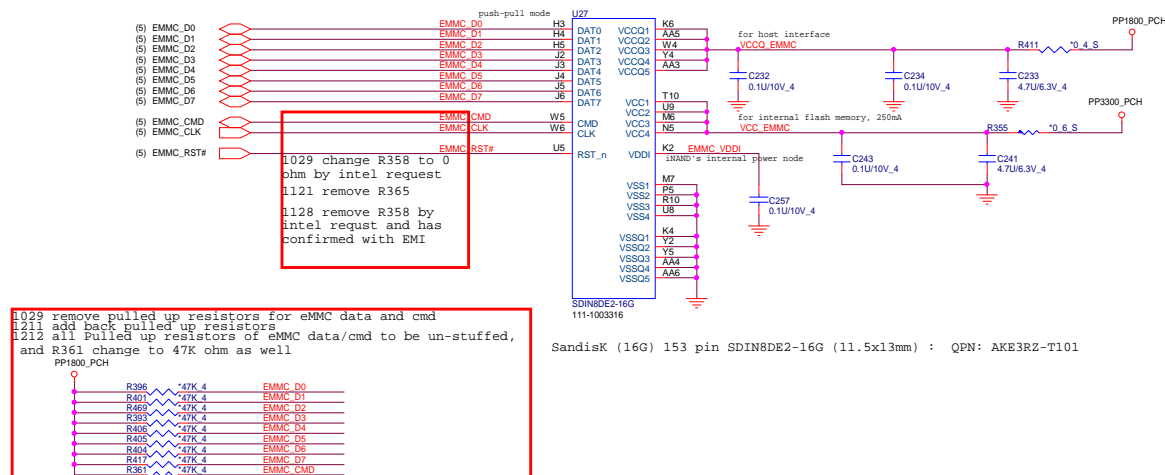
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1025 Delete complete SSD(connector and caps)

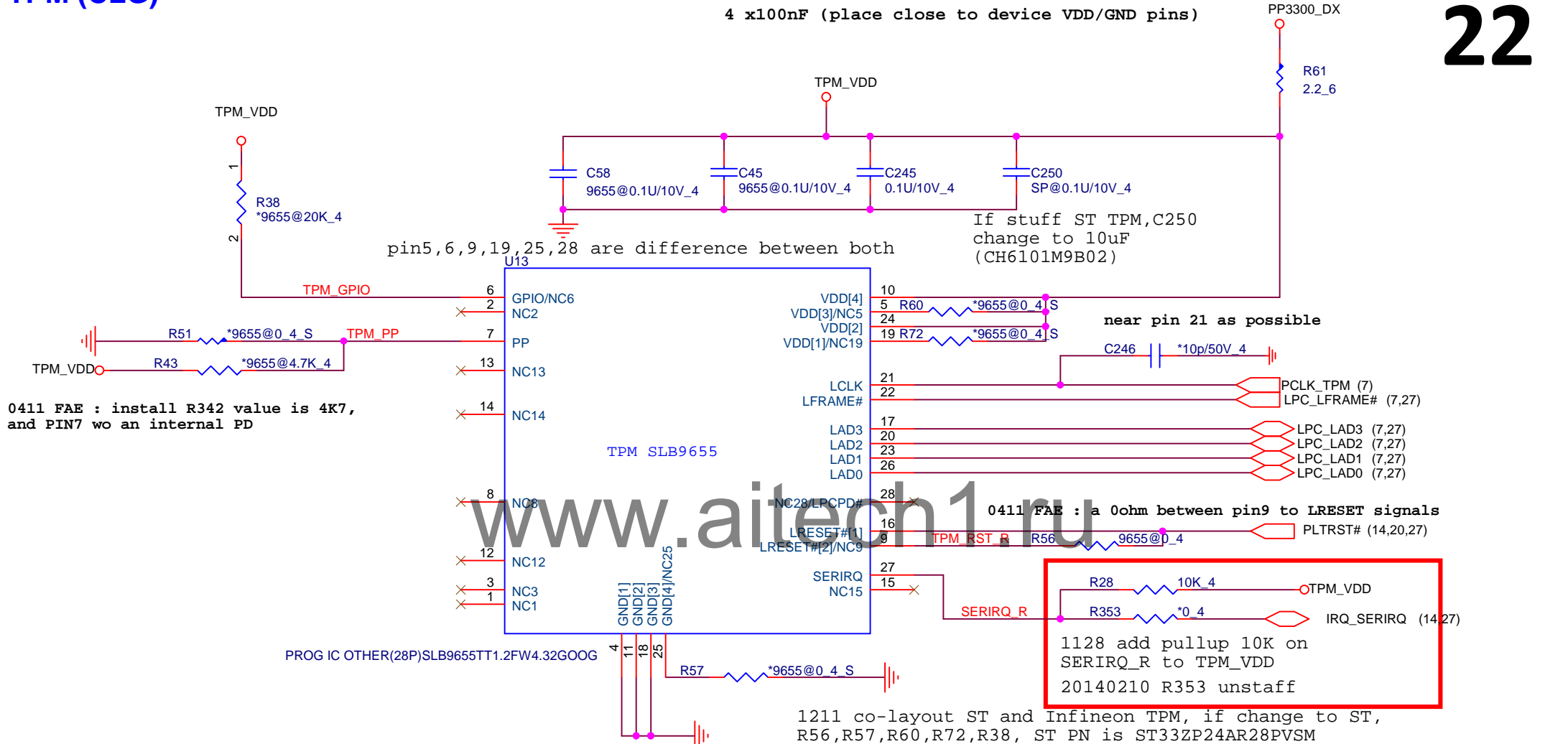
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EMMC (CBS)

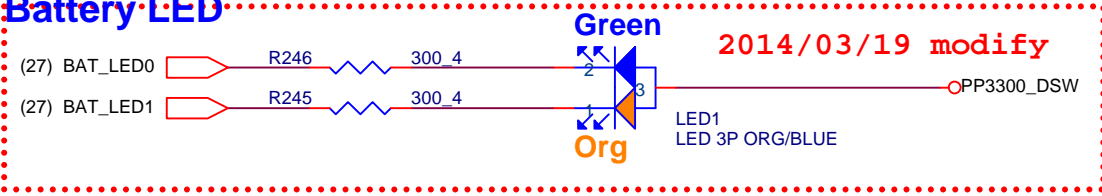


TPM (CLG)


22



LED(UIF) Battery LED



0319 Del Power LED

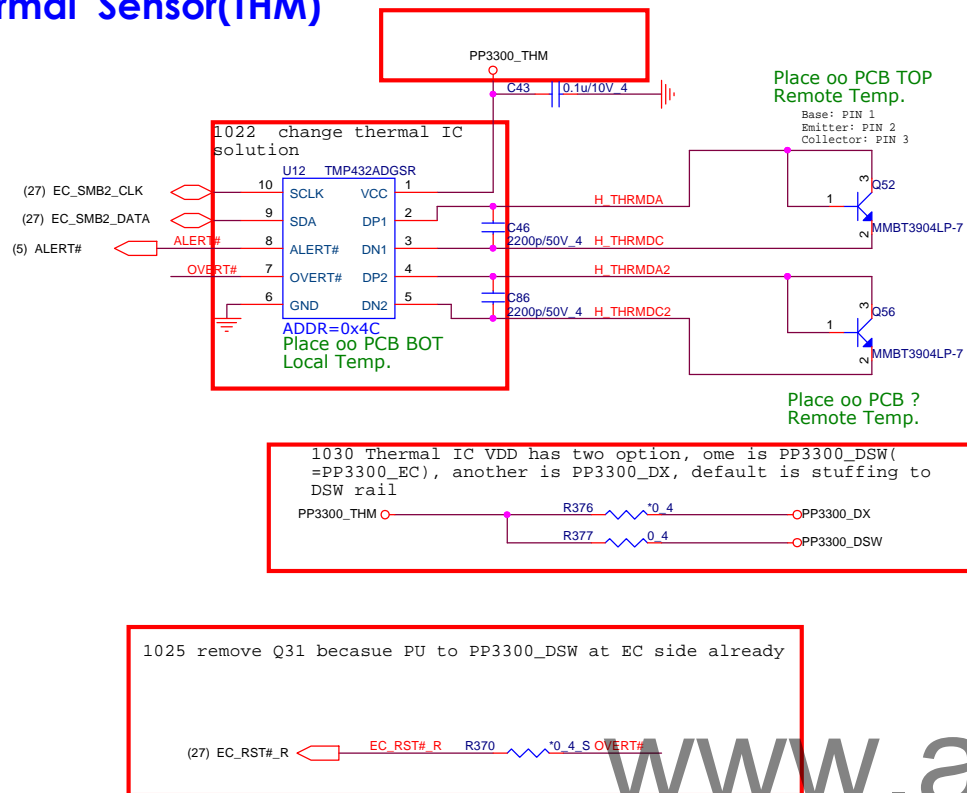


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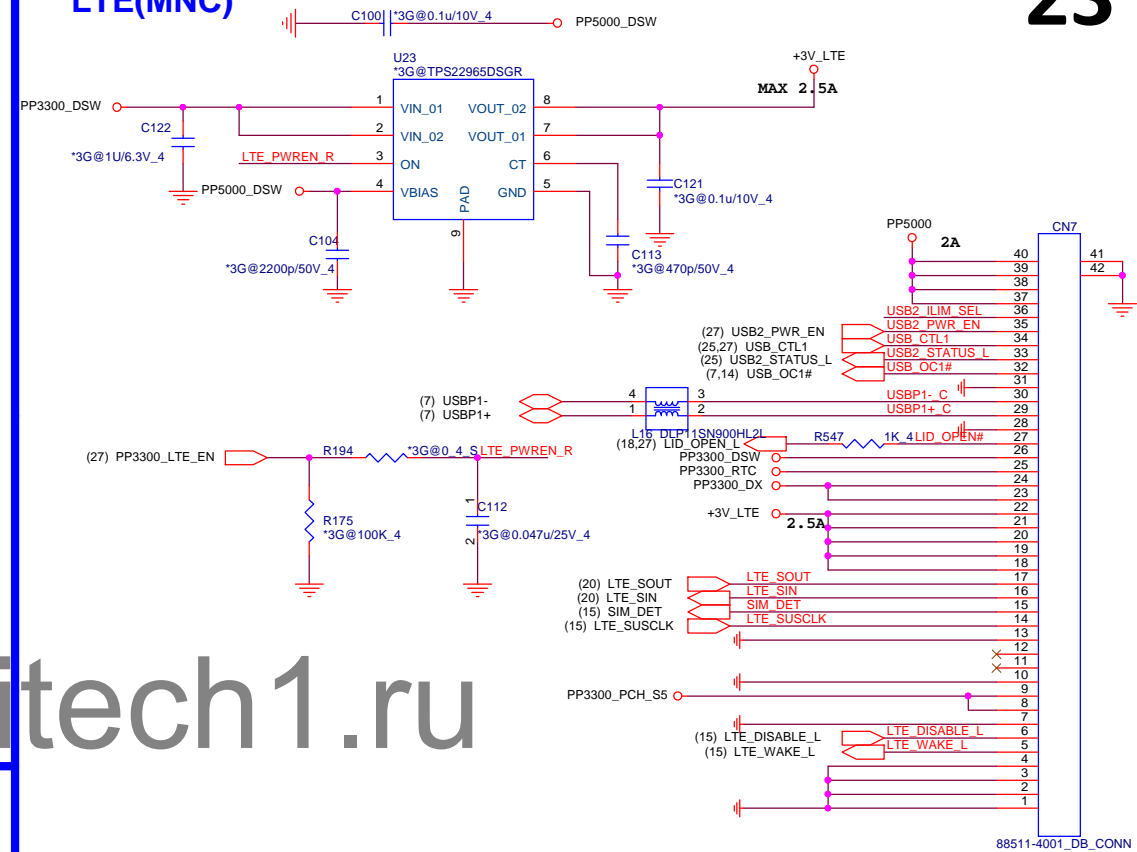
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| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | TPM SLB9655 / LED | 1A |
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Thermal Sensor(THM)

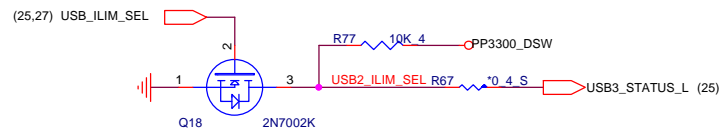



FUNCTION DB LTE(MNC)



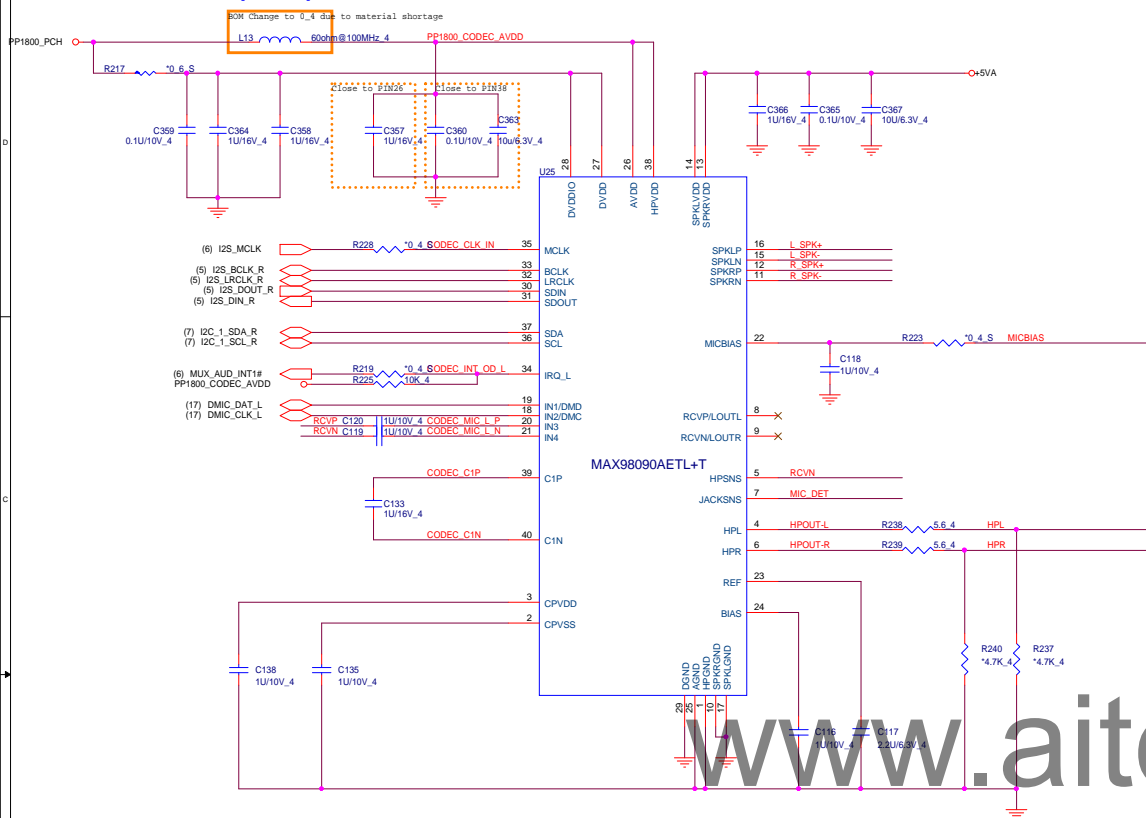
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USB Switch Current Control

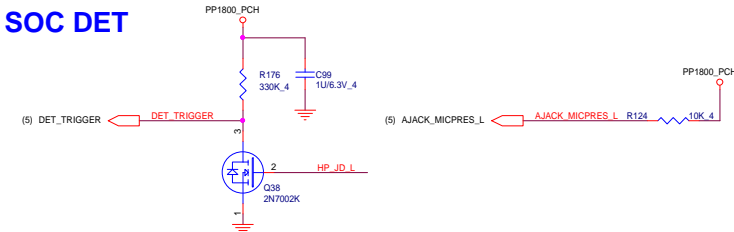


| | | | | |
|--|------------------------|-------|------------------------------|-------|
|  Quanta Computer Inc. PROJECT : NL6 | | Size | Document Number | Rev |
| | | | DB/ALS/Thermal sensor | 1A |
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AUDIO CODEC (ADO)



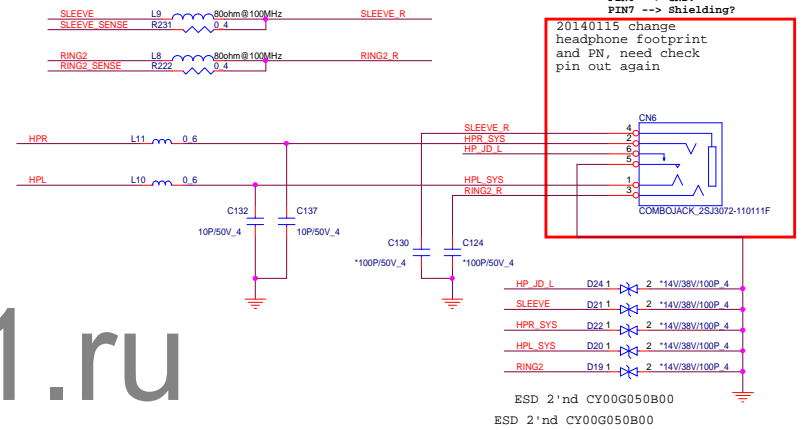
SOC DET



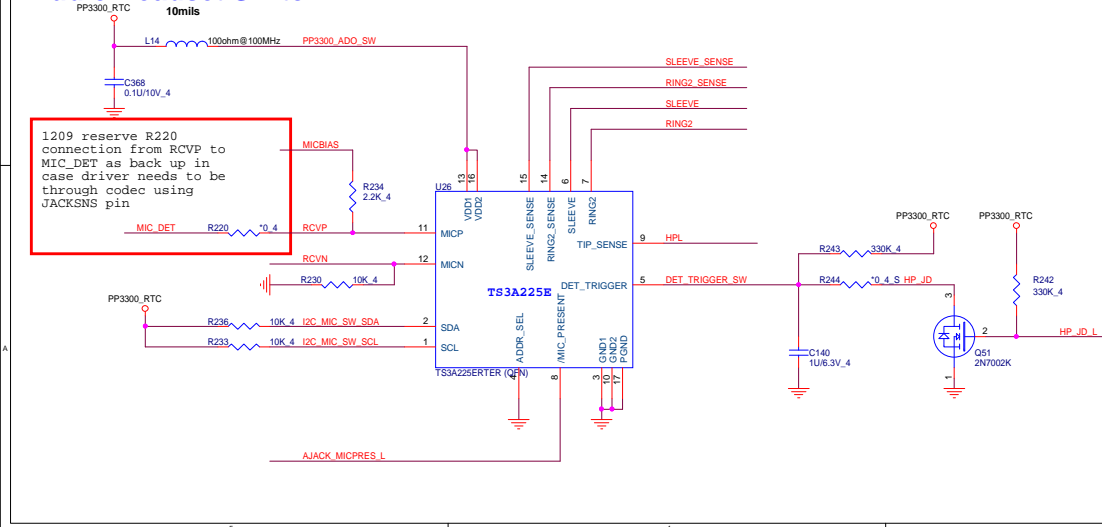
HEADPHONE/Mic combo(ADO)

combo jack
Normal open

P/N: DFTJ06FR652
Normal Open
PIN1 --> L?
PIN2 --> R?
PIN3 --> GND/MIC?
PIN4 --> MIC/GND?
PIN5 --> JD?
PIN6 --> GND?
PIN7 --> Shielding?



Audio Headset Switch

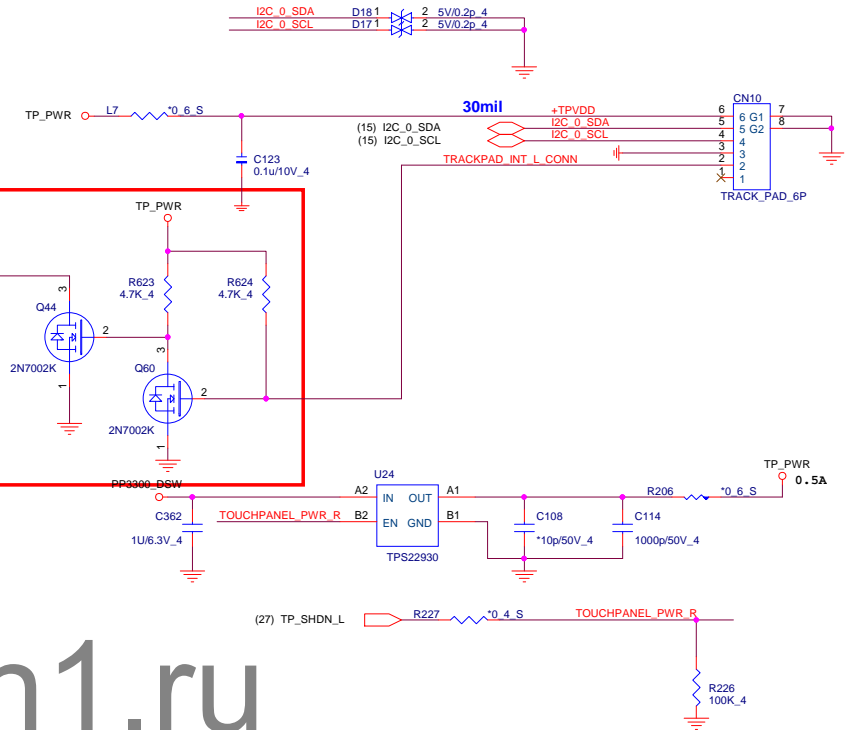
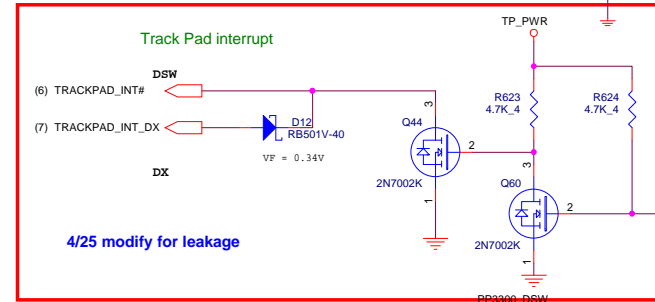
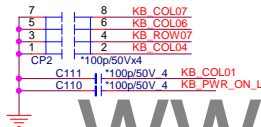
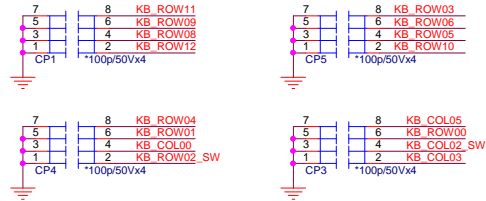
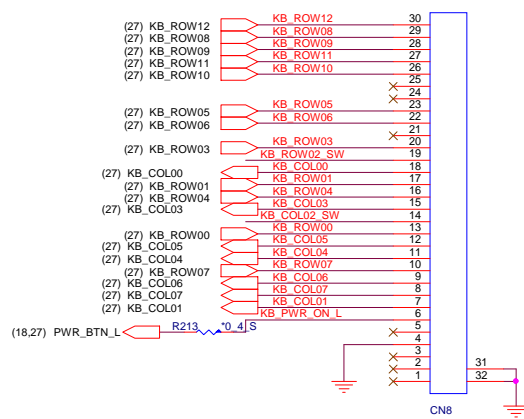


Track PAD BOARD CONN (TPD)

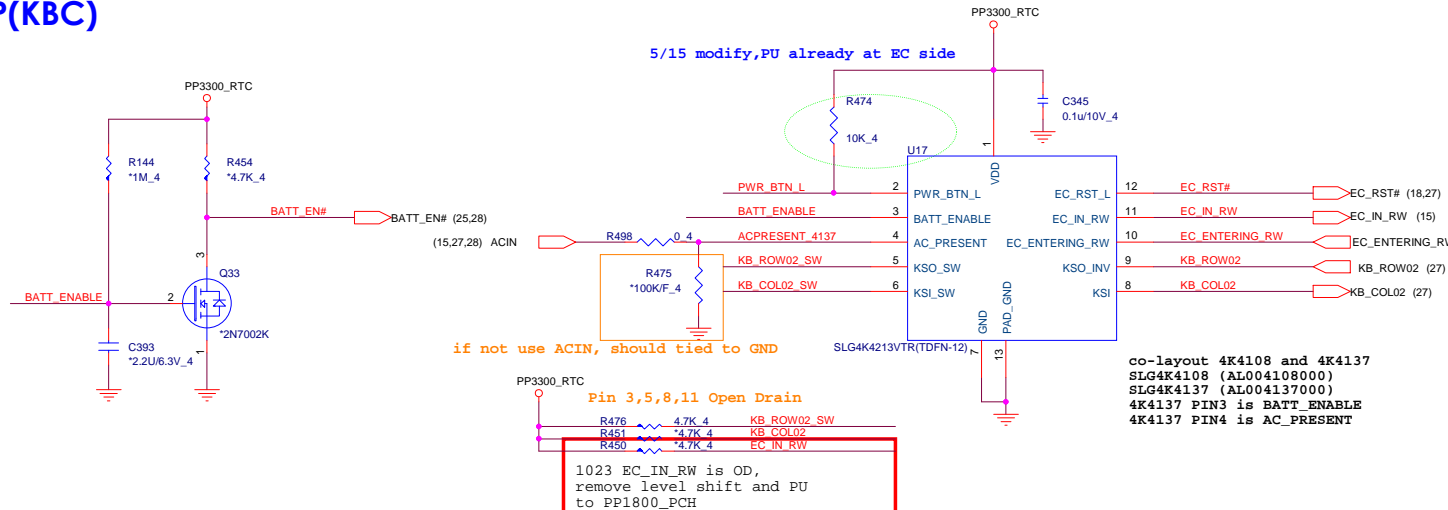
K/B (KBC)

20140127 Change KB CONN for ME require

KB_CONN_51518-03001-001



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HOLELESS RESET
2-CHIP(KBC)

Connect to EC reset pin
Connect to GPIO on CPU
with PU to GPIO power
well
Connect to EC pin C5 (must
be low when EC IN RESET)

co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

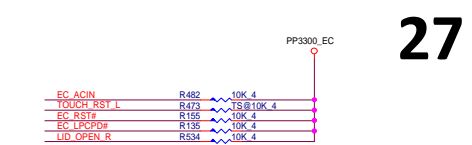


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| Size | Document Number | Rev |
|------|--------------------|-----|
| | KB/TP/FAN/HW Reset | 1A |

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BATT and CHARGER / LCD BL

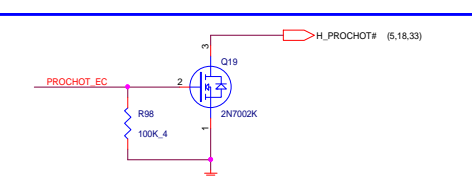
BATT and CHARGER / LCD BU

| | |
|--------------|------|
| EC_SMB0_CLK | R419 |
| EC_SMB0_DATA | R422 |

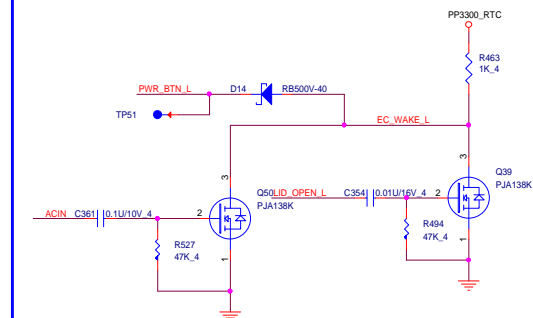
1030 Thermal IC VDD has two option, ome is
PP3300_DSW(=PP3300_EC), another is
PP3300_DX, default is stuffing to DSW rail

THERMAL SENSOR

| | | |
|--------------|------|--|
| EC_SMB2_CLK | R140 | |
| EC_SMB2_DATA | R132 | |



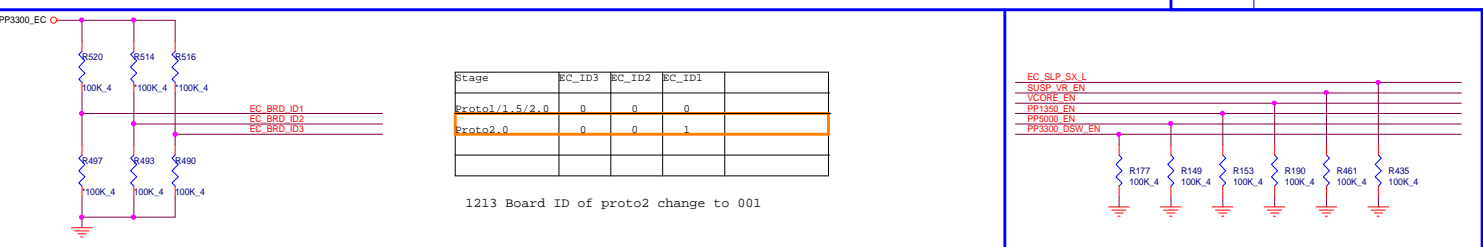
EC HIB WAKE SOURCES



SM BUS ARRANGEMENT TABLE

| | |
|----------|------------------|
| SM Bus 0 | BATT and CHARGER |
| SM Bus 1 | NA |
| SM Bus 2 | THERMAL SENSOR |
| | |

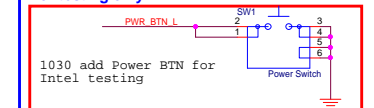
1211 add Test points on unused pins, need check layout to see if all points are ok

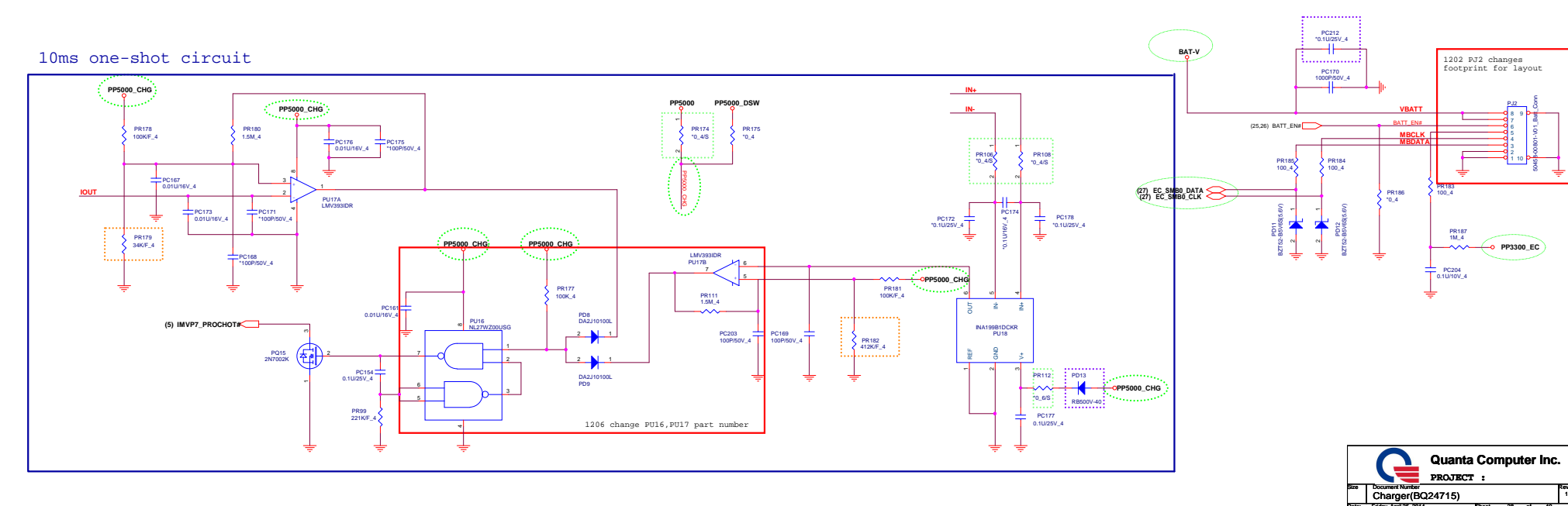


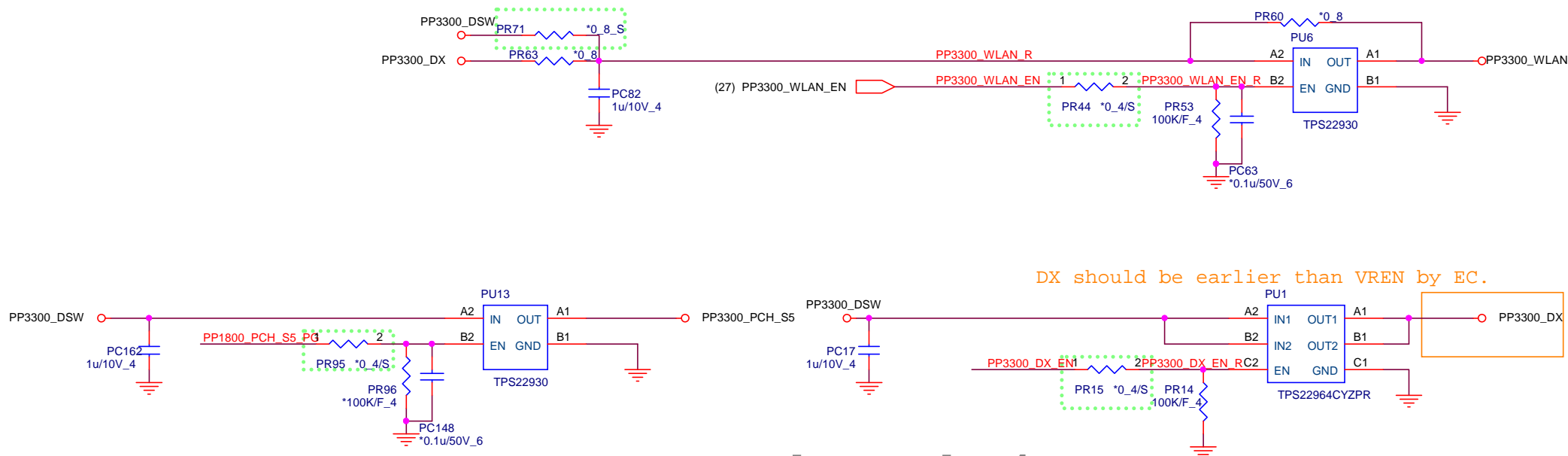
OD pin list

EC_REST_L
BAT_LED0
BAT_LED1
PCH_RSMRST_L
SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L

For testing only







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PROJECT :

| | | |
|-------|---------------------------------------|----------------|
| Size | Document Number Load Switch | Rev 1A |
| Date: | Friday, April 25, 2014 | Sheet 30 of 40 |

TDC : 0.75A
PEAK : 1A
Width : 10mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

Greater than or equal 40mil

0417 PC13 change to 10uF ,
add 2x10uF PC215 , PC216

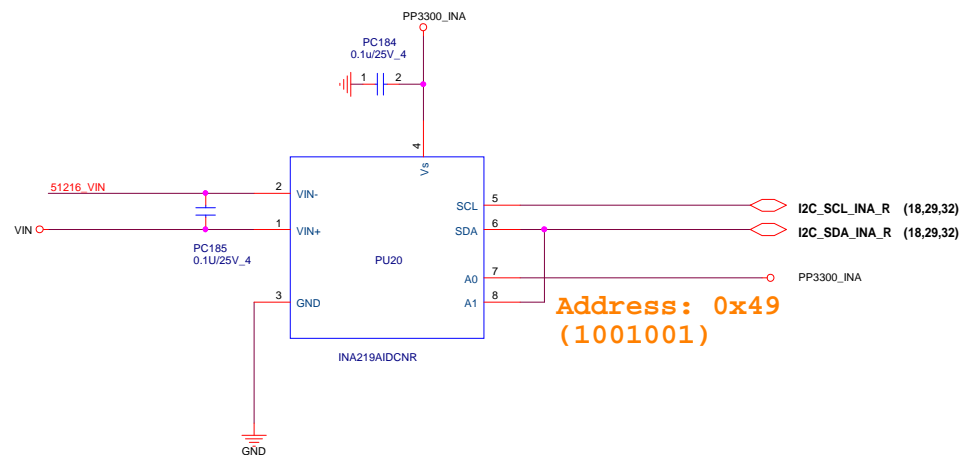
1.35 Volt +/- 5%
TDC : 3.55A
PEAK : 4.73A
OCP : 6A
Width : 160mil

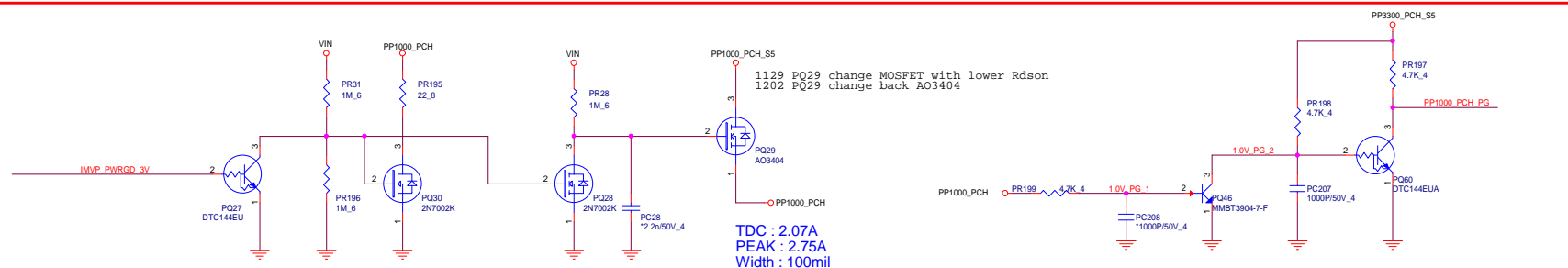
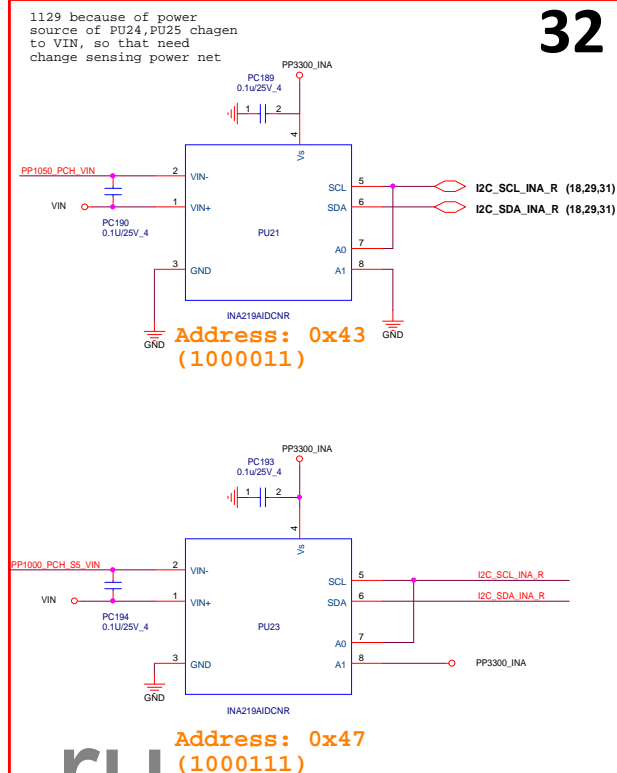
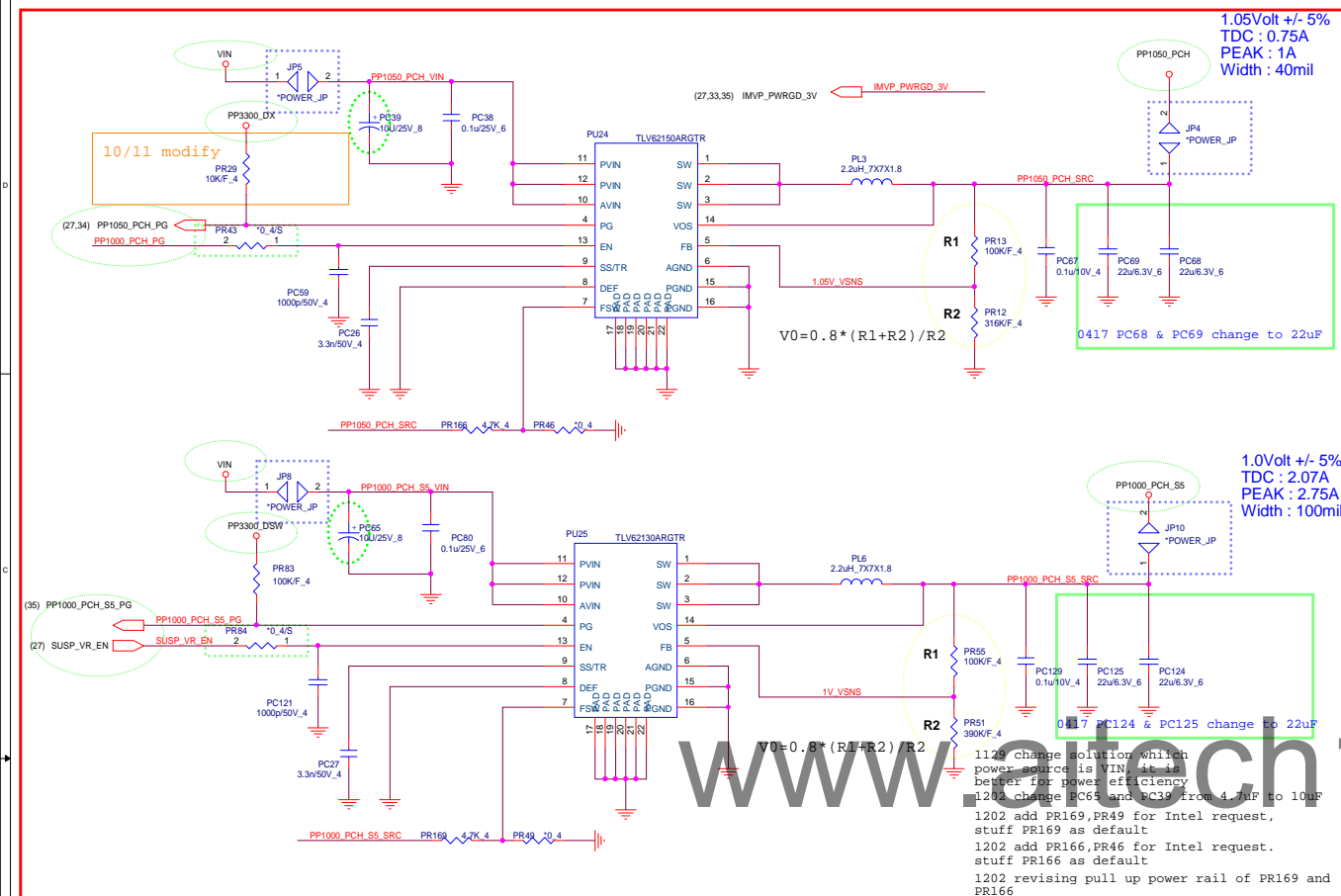
www.aitech1.ru

OCP=6A
L ripple current
= $(19-1.35) \times 1.35 / (2.2 \times 400 \times 19)$
=1.425A
 $V_{trip} = [6 - (1.425/2)] \times 14 \text{mohm}$
=0.07402V
 $R_{limit} = 0.07402 / 10 \mu A \times 8 = 59.22 \text{Kohm}$

| Mode | Frequency | Discharge mode |
|------|-----------|--------------------|
| 200K | 400K | Tracking Discharge |
| 100K | 300K | Tracking Discharge |

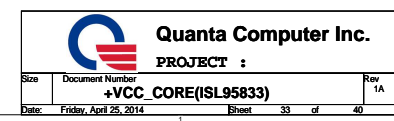
| | S3 | S5 | +1.35VSUS | REF | VTT |
|------------------|----|----|-----------|-----|-----|
| S0 | 1 | 1 | ON | ON | ON |
| S3 (main on off) | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |





1129 PP1000_PCH changes from convert to power MOSFET type for power efficiency improvement

0417 PC87 &
PC88 change to
10uF



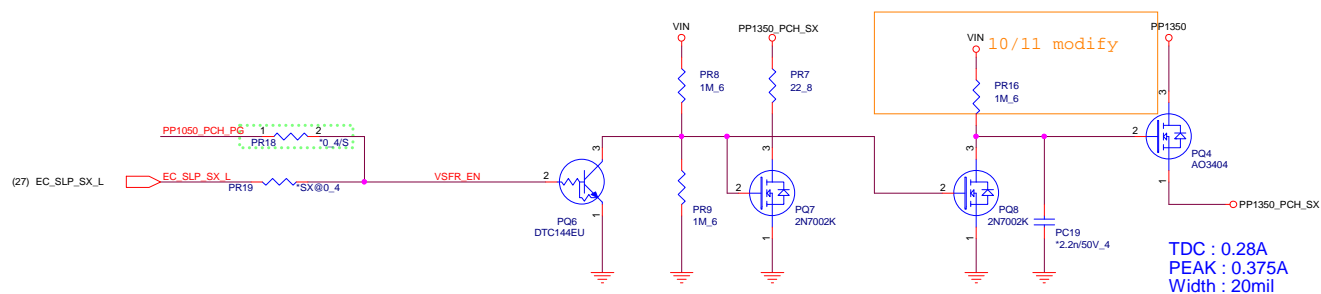
www.ait

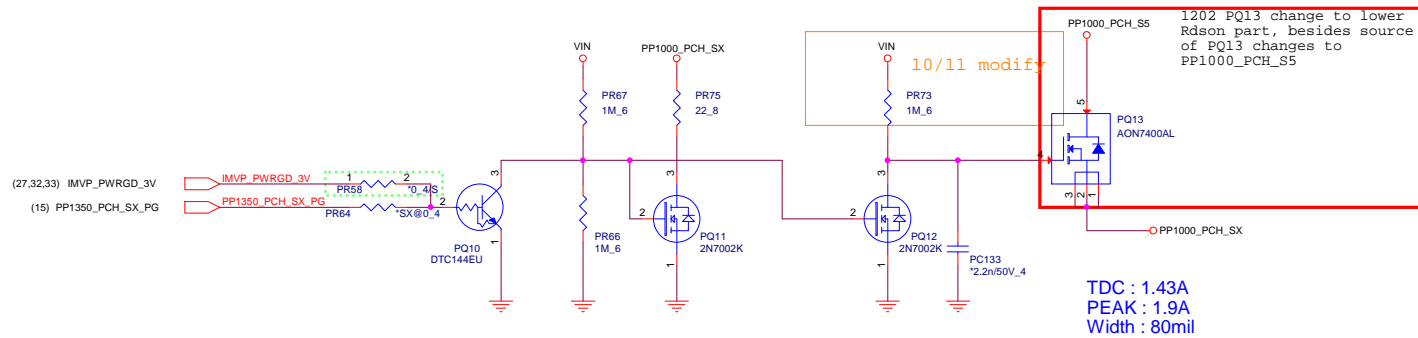
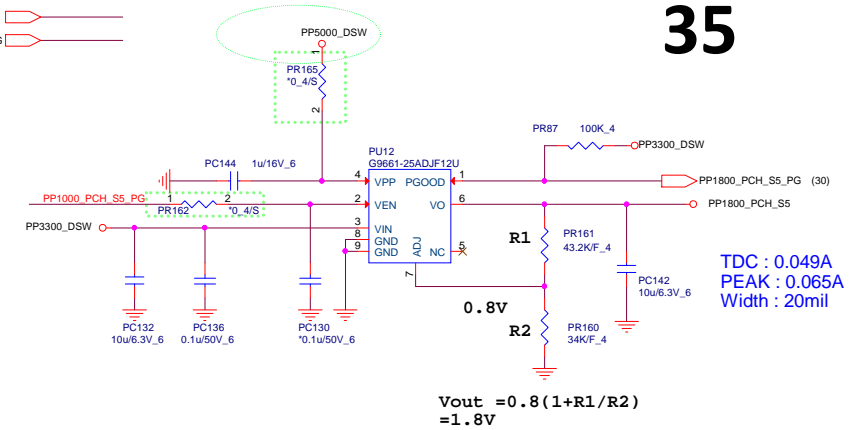
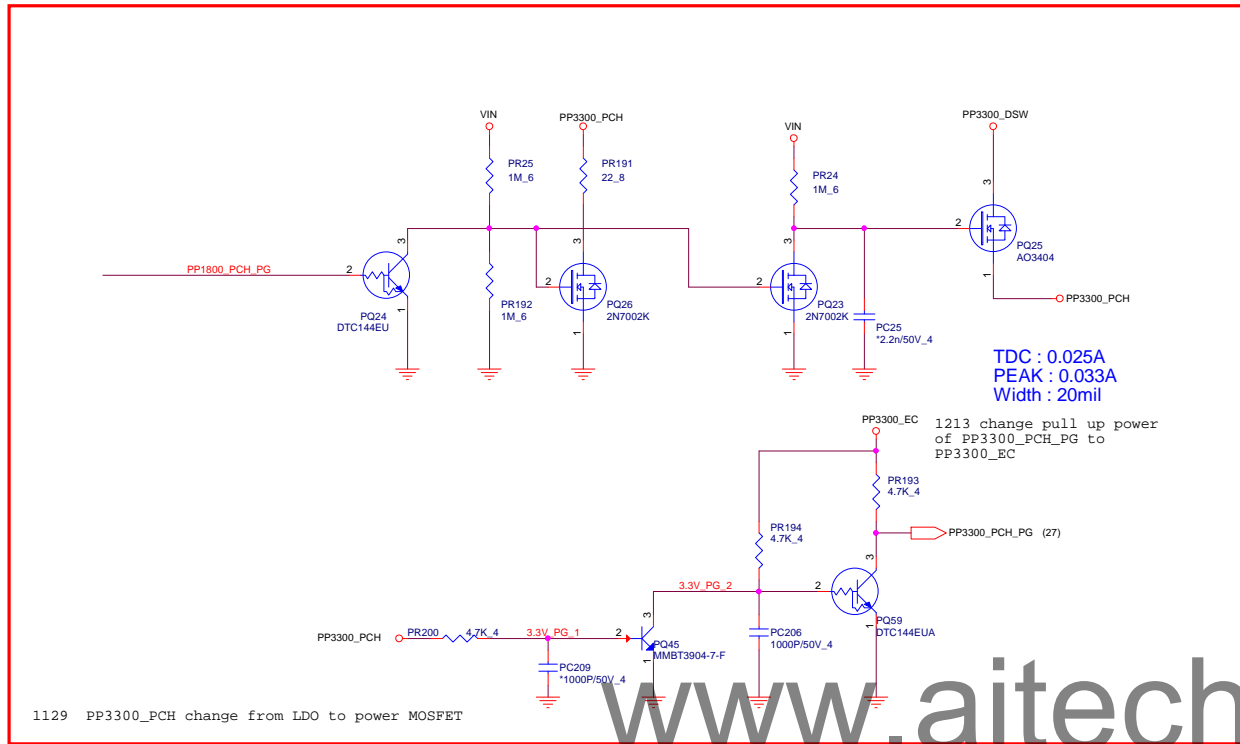
The schematic shows a voltage divider circuit powered by PP3300_DSW. The input voltage is divided by resistors R1 (100K_4) and R2 (34K_F_4) to provide 0.8V to the GND pin of the PU19 G9681-25ADJF12U regulator. The regulator's VPP pin is connected to the output of the divider, and its PGOOD pin is connected to PP1800_PCH_PG. The output of the regulator is connected to PP1800_PCH_PG (35). The circuit also includes decoupling capacitors PC182, PC181, PC183, and PC180.

$$V_{out} = 0.8(1 + R1/R2)$$

$$= 1.8V$$

TDC : 0.026A
PEAK : 0.035A
Width : 20mil





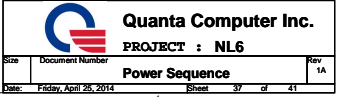
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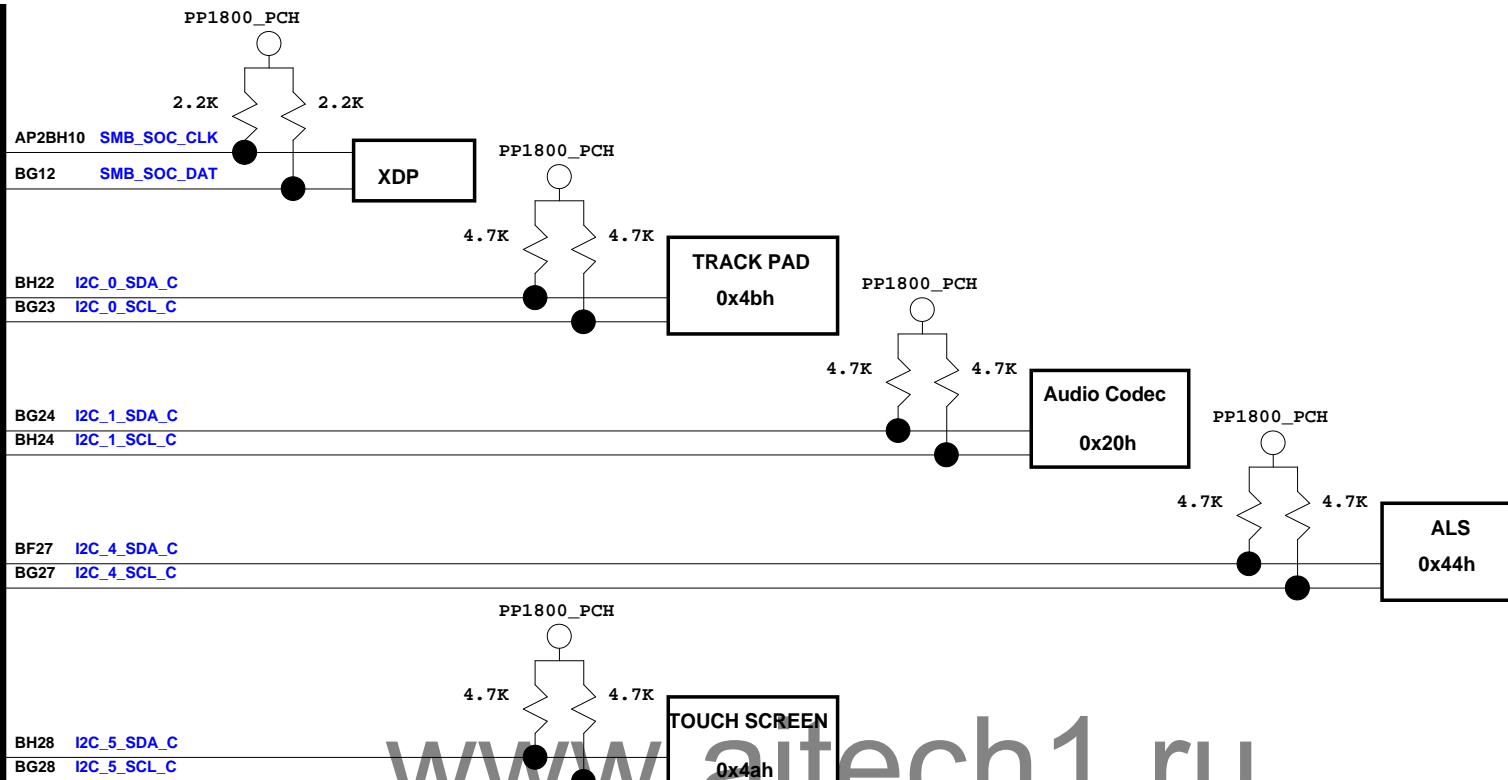
PROJECT :

| | | |
|-------|------------------------|----------------|
| Size | Document Number | Rev |
| | Thermal protect | 1A |
| Date: | Friday, April 25, 2014 | Sheet 36 of 41 |

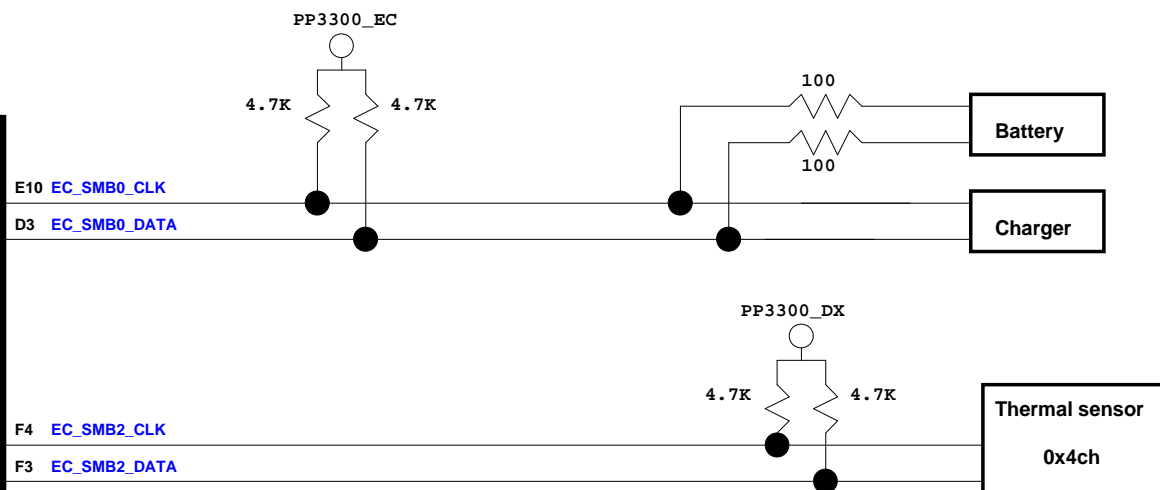


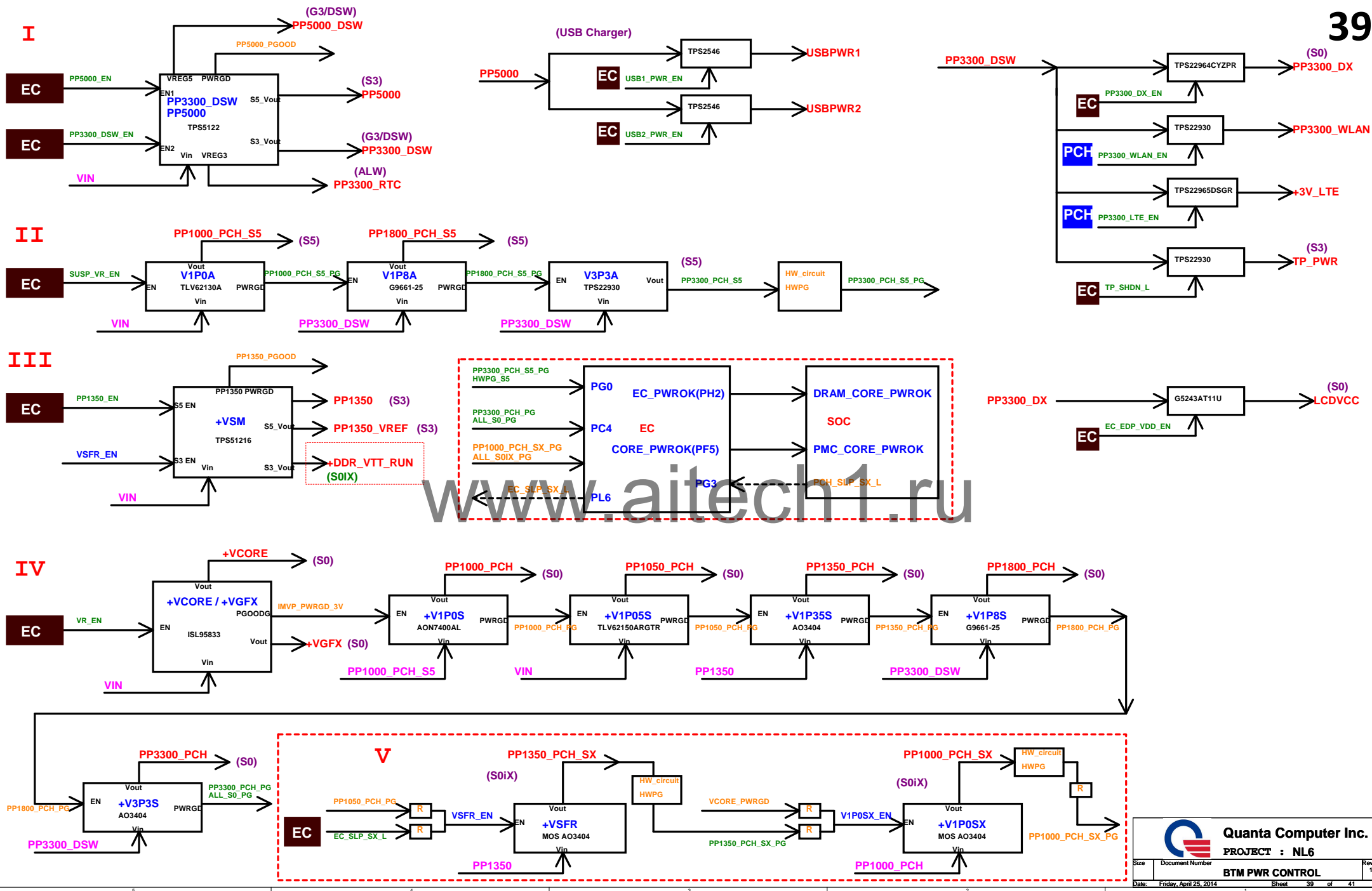
SMBUS
Bay-trail M


I2C



KBC
TI
SMBUS





| | | |
|--|------------------------|----------------|
|  Quanta Computer Inc. PROJECT : 0C2A | | |
| Size | Document Number | Rev |
| Change list-2 | | 1 |
| Date: | Friday, April 25, 2014 | Sheet 41 of 41 |